



# AMT: a Property-based Tool for Monitoring Analog Systems

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# Overview

- Introduction
- STL/PSL Specification Language
  - ❖ Analog Layer
  - ❖ Temporal Layer
  - ❖ Distance-based Operators
- Checking STL/PSL Properties
  - ❖ Offline Marking
  - ❖ Incremental Marking
- AMT Tool
- FLASH Memory Case Study

# Introduction

- Verification of discrete systems
  - ❖ Model checking TL specs
  - ❖ Central role in algorithmic verification
  - ❖ Efficient algorithms for LTL, CTL, PSL etc.
- Verification of real-time systems
  - ❖ Emptiness checking of *timed automata*
    - KRONOS, UPPAAL, IF etc.
  - ❖ Many variants of real-time logics
    - MTL, MITL, TCTL etc.
  - ❖ Only TCTL used in a real-time verification tool
- Lightweight verification
  - ❖ Systems may be too complex to verify exhaustively
    - Software
    - Very large digital systems
    - Many real-time systems etc.
  - ❖ Property monitors
    - Generated automatically from the specification
    - Observe individual simulation traces and check whether the property is violated
    - Incomplete but more reliable method than manual visual inspection of simulation traces

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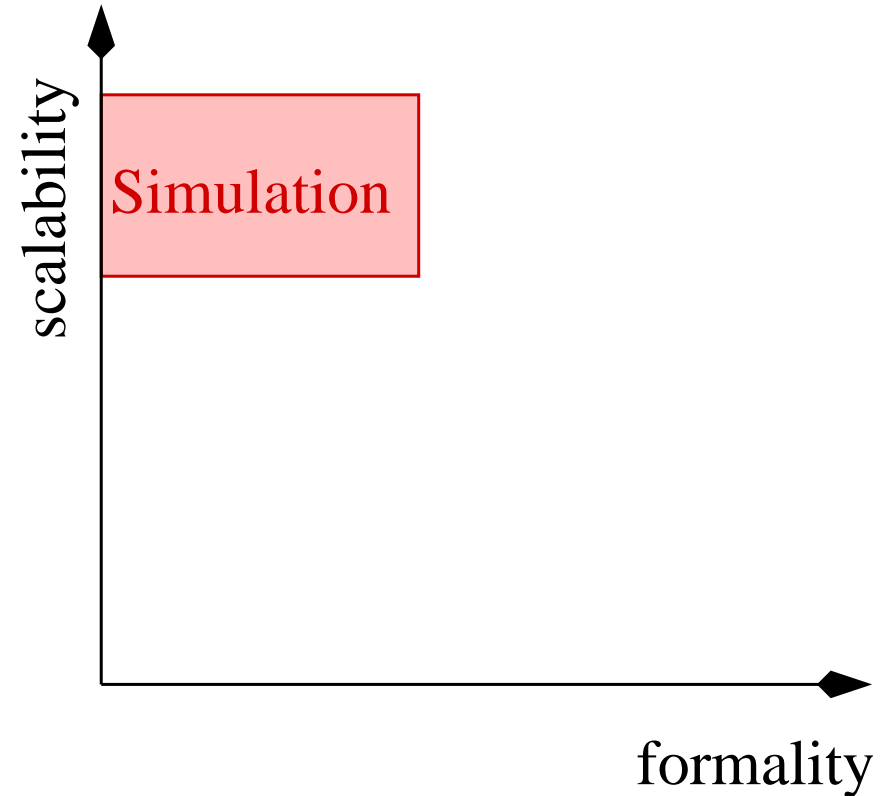
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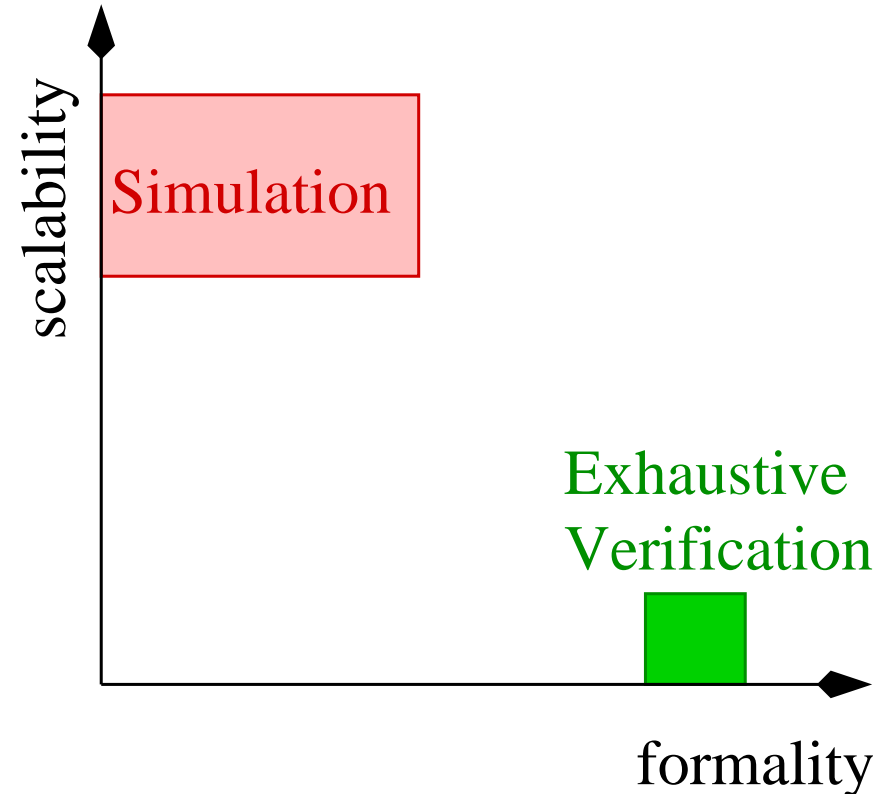
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- Verification of continuous systems
  - ❖ Manual inspection of simulation traces
    - Dominant technique
    - Requires experienced specialists
    - Error prone
  - ❖ Exhaustive analog verification
    - Powerful formalisms such as hybrid automata
    - Limited scalability
- **Our approach:** Property-based lightweight verification of continuous signals



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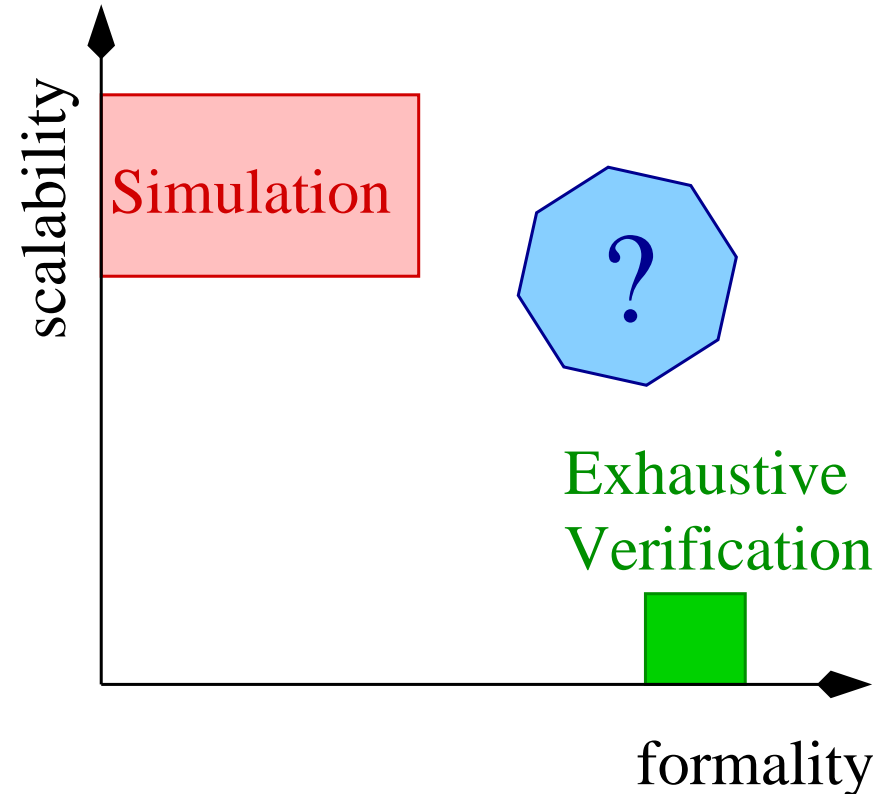
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# Signals

- Finite length signal  $\xi$  defined over an abstract domain  $\mathbb{D}$ 
  - ❖ Partial function  $\xi : \mathbb{T} \rightarrow \mathbb{D}$
  - ❖ Length of  $\xi$  is  $r$  ( $|\xi| = r$ )
  - ❖  $\xi[t] = \perp$  when  $t \geq |\xi|$
  - ❖ **Boolean signals:**  $(\xi_b) \mathbb{D} = \mathbb{B}$
  - ❖ **Continuous signals:**  $(\xi_a) \mathbb{D} = \mathbb{R}$
- **Restriction** of a signal  $\xi$  to length  $d$

$$\xi' = \langle \xi \rangle_d \text{ iff } \xi'[t] = \begin{cases} \xi[t] & \text{if } t < d \\ \perp & \text{otherwise} \end{cases}$$

- **Concatenation**  $\xi = \xi_1 \cdot \xi_2$

$$\xi[t] = \begin{cases} \xi_1[t] & \text{if } t < r_1 \\ \xi_2[t - r_1] & \text{otherwise} \end{cases}$$

- **$d$ -suffix** of a signal  $\xi$ ,  $\xi' = d \setminus \xi$

$$\xi'[t] = \xi[t + d] \quad \text{for every } t \in [0, |\xi| - d)$$

# Signals

- **Minkowski sum** and **difference** of two sets  $P_1$  and  $P_2$  are defined as

$$P_1 \oplus P_2 = \{x_1 + x_2 : x_1 \in P_1, x_2 \in P_2\}$$
$$P_1 \ominus P_2 = \{x_1 - x_2 : x_1 \in P_1, x_2 \in P_2\}.$$

- **Projection** of the signal  $\xi$  on the dimension with domain  $\mathbb{B}$  which corresponds to the proposition  $p$ ,  $\xi_p = \pi_p(\xi)$ 
  - ❖ Likewise  $\xi_s = \pi_s(\xi)$  is the projection of the signal  $\xi$  on the dimension with domain  $\mathbb{R}$  which corresponds to the continuous variable  $s$
- **Signal representation**
  - ❖ Boolean signals:
    - Non-Zeno finite length signals admit finite representation
    - Sequence of adjacent intervals with value constant in each interval
  - ❖ Continuous signals:
    - Do not admit an exact finite representation
    - But, numerical simulators produce a **finite** collection of sampling points
    - The signal value at missing points in time is interpolated

# STL/PSL *Specification Language*

- Extension of real-time temporal logic MITL with analog constructs
- PSL-like layered approach
  - ❖ **Analog layer:** allows reasoning about continuous signals
  - ❖ **Temporal layer:** relates the temporal behavior of input traces
- “Communication” between two layers via **static abstractions**
  - ❖ Partitioning of the continuous state space according to the satisfaction of some inequality constraints on the continuous variables
- Targeted to be used in *lightweight* verification
  - ❖ PSL-like **finitary interpretation** of temporal operators

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# STL/PSL: *Analog Layer*

- **Syntax:**

$$\phi ::= s \mid \text{shift}(\phi, k) \mid \phi_1 \star \phi_2 \mid \phi \star c \mid \text{abs}(\phi)$$

where  $s$  belongs to a set  $S = \{s_1, s_2, \dots, s_n\}$  of continuous variables,  $\star \in \{+, -, *\}$ ,  $c \in \mathbb{Q}$  and  $k \in \mathbb{Q}^+$ .

- **Semantics:**

$$\begin{aligned} s[t] &= \pi_s(\xi)[t] \\ \text{shift}(\phi, k)[t] &= \phi[t + k] \\ (\phi_1 \star \phi_2)[t] &= \phi_1[t] \star \phi_2[t] \\ (\phi \star c)[t] &= \phi[t] \star c \\ \text{abs}(\varphi)[t] &= \begin{cases} \phi[t] & \text{if } \phi[t] \geq 0 \\ -\phi[t] & \text{otherwise} \end{cases} \end{aligned}$$

- Pragmatic choice of analog operators

- ❖ Based on the feedback of analog designers
- ❖ Can be naturally extended



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# STL/PSL: *Temporal Layer*

- **Syntax:**

$$\begin{aligned} \varphi ::= & p \mid \phi \circ c \mid \text{not } \varphi \mid \varphi_1 \text{ or } \varphi_2 \mid \text{eventually! } \varphi \mid \\ & \text{eventually!}[a:b] \varphi \mid \text{eventually}[a:b] \varphi \mid \\ & \varphi_1 \text{ until! } \varphi_2 \mid \varphi_1 \text{ until!}[a:b] \varphi_2 \end{aligned}$$

where  $p$  belongs to a set  $P = \{p_1, p_2, \dots, p_n\}$  of propositional variables,  $a, b, c \in \mathcal{Q}$  and  $\circ \in \{>, \geq, <, \leq\}$ .

- **Semantics:** The satisfaction relation  $(\xi, t) \models \varphi$ , indicating that signal  $\xi$  satisfies  $\varphi$  at time  $t$  is defined inductively as follows:

$$\begin{aligned} (\xi, t) \models \text{eventually! } \varphi & \quad \text{iff} \quad \exists t' \geq t \text{ st } t' < |\xi| \text{ and } (\xi, t') \models \varphi \\ (\xi, t) \models \text{eventually!}[a:b] \varphi & \quad \text{iff} \quad \exists t' \in t \oplus [a, b] \text{ st } t' < |\xi| \text{ and } (\xi, t') \models \varphi \\ (\xi, t) \models \varphi_1 \text{ until! } \varphi_2 & \quad \text{iff} \quad \exists t' \geq t \text{ st } t' < |\xi| \text{ and } (\xi, t') \models \varphi_2 \text{ and} \\ & \quad \forall t'' \in [t, t'] (\xi, t'') \models \varphi_1 \\ (\xi, t) \models \varphi_1 \text{ until!}[a:b] \varphi_2 & \quad \text{iff} \quad \exists t' \in t \oplus [a, b] \text{ st } t' < |\xi| \text{ and } (\xi, t') \models \varphi_2 \text{ and} \\ & \quad \forall t'' \in [t, t'] (\xi, t'') \models \varphi_1 \end{aligned}$$

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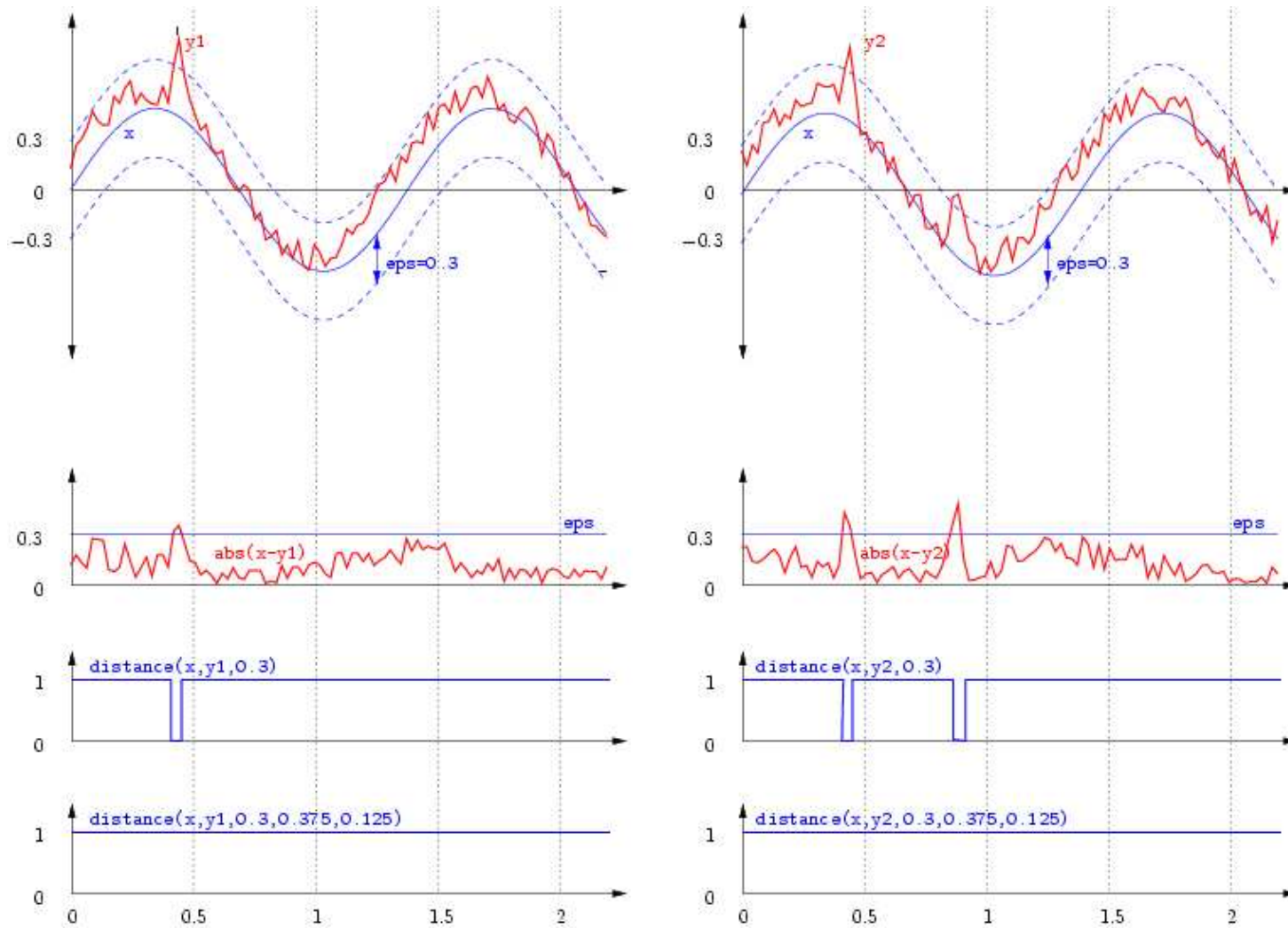
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## STL/PSL: *Distance-based Operators*

- **Motivation:** Enrich STL/PSL with **metric properties**
- Compare waveforms with some reference signal that specifies a desired behavior
- Distance function (metric)
  - ❖ Quantifies numerically the resemblance of two signals

$$\begin{aligned} \text{distance}(\phi_1, \phi_2, c) &= \text{abs}(\phi_1 - \phi_2) \leq c \\ \text{distance}(\phi_1, \phi_2, c, t, T) &= \text{abs}(\phi_1 - \phi_2) > c \rightarrow \text{eventually!}[\leq t] \\ &\quad \text{always}[\leq T-t](\text{abs}(\phi_1 - \phi_2) \leq c) \\ \text{distance}(\varphi_1, \varphi_2, t, T) &= (\varphi_1 \text{ xor } \varphi_2) \rightarrow \text{eventually!}[\leq t] \\ &\quad \text{always}[\leq T-t](\varphi_1 \text{ iff } \varphi_2) \end{aligned}$$

# STL/PSL: Distance-based Operators Example



# Checking STL/PSL Properties

- **Marking:** a procedure that determines the truth values of each subformula of an STL/PSL specification at every time instant  $t$ 
  - ❖ Doubly-recursive procedure, on time and the structure of the formula
- Two algorithms for checking STL/PSL properties:
  - ❖ **Offline marking:** input is fully available
  - ❖ **Incremental marking:** input is dynamically observed
- Based on [MalerN04]

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# Offline Marking

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input : STL/PSL Temporal Formula  $\varphi$  and signal  $\xi$ 
switch  $\varphi$  do
  case  $p$ 
    |  $\chi_\varphi := \pi_p(\xi);$ 
  end
  case  $OP_2(\varphi_1, \varphi_2)$ 
    | OFFLINE ( $\varphi_1, \varphi_2$ );
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- Inputs:
  - ❖ Multidimensional signal  $\xi$
  - ❖ STL/PSL specification  $\varphi$
- Compute, from **bottom-up**, a signal  $\chi_\psi(\xi)$  for each subformula  $\psi$  of  $\phi$
- COMBINE computes from input signals a new signal based on the specific operation

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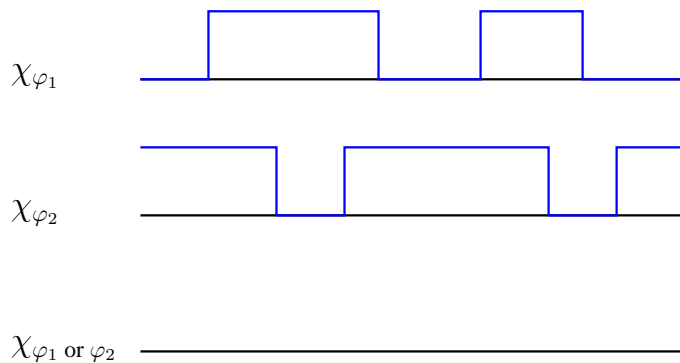
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# COMBINE: *Disjunction and Eventually*

## ● Disjunction

- ❖ Refine the intervals of  $\chi_{\phi_1}$  and  $\chi_{\phi_2}$  so that the mutual values of both signals become uniform in every interval
- ❖ Compute the disjunction interval-wise
- ❖ Merge the adjacent intervals having the same value



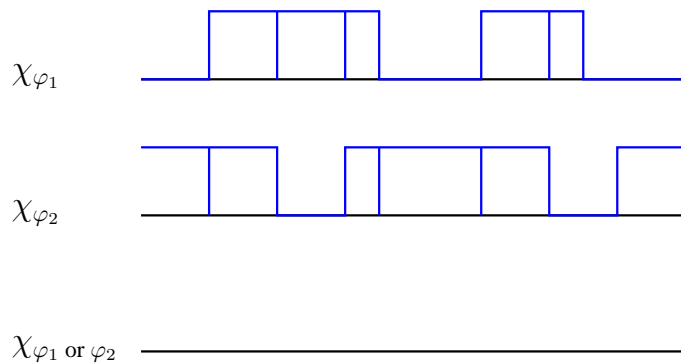
## ● Bounded Eventually

- ❖ For every positive interval  $I \in \chi_{\phi_1}$
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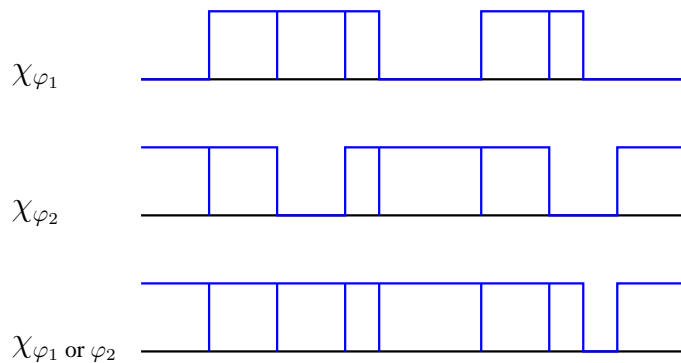
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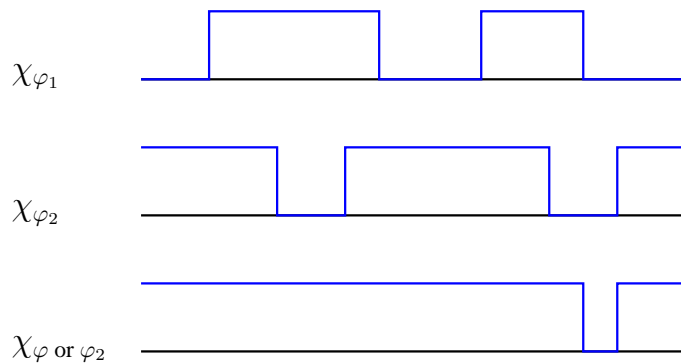
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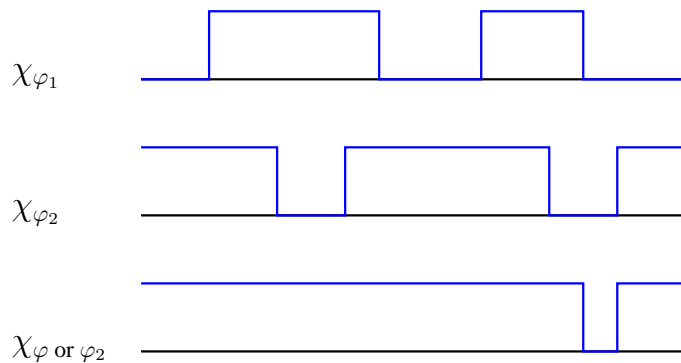
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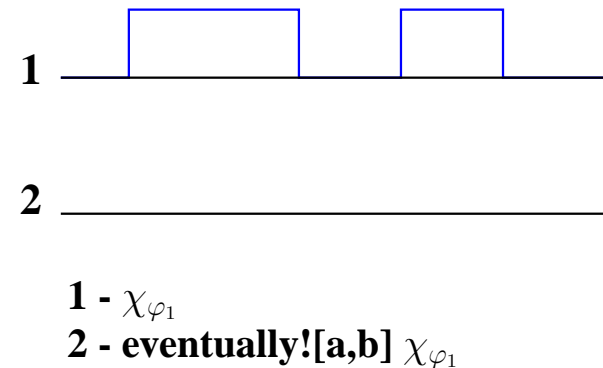
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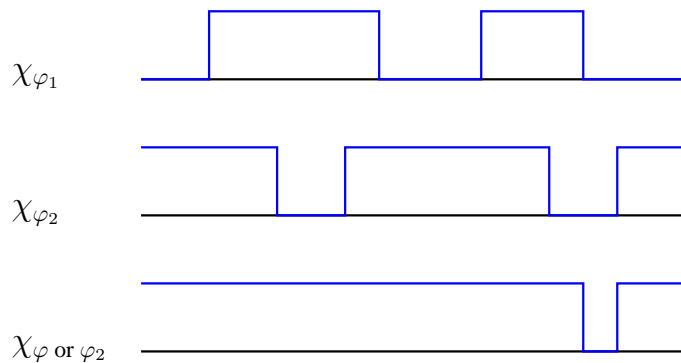
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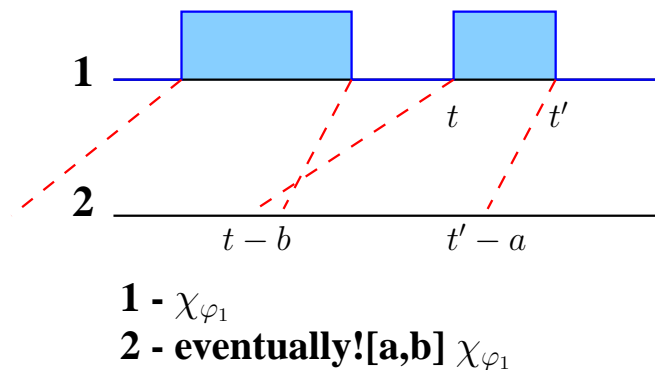
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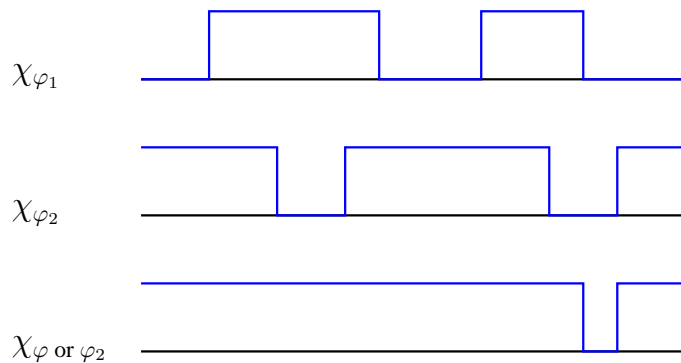
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- ❖ Compute its **back shifting**  $I - [a, b] \cap \mathbb{T}$
- ❖ Merge the overlapping intervals in  $\chi_{\phi}$



# COMBINE: *Disjunction and Eventually*

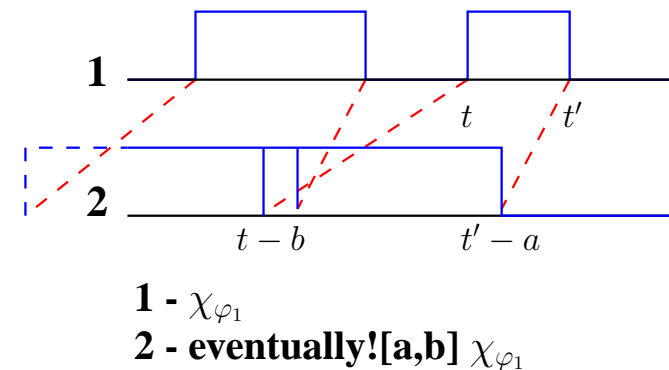
- Disjunction

- ◆ Refine the intervals of  $\chi_{\phi_1}$  and  $\chi_{\phi_2}$  so that the mutual values of both signals become uniform in every interval
- ◆ Compute the disjunction interval-wise
- ◆ Merge the adjacent intervals having the same value



- Bounded Eventually

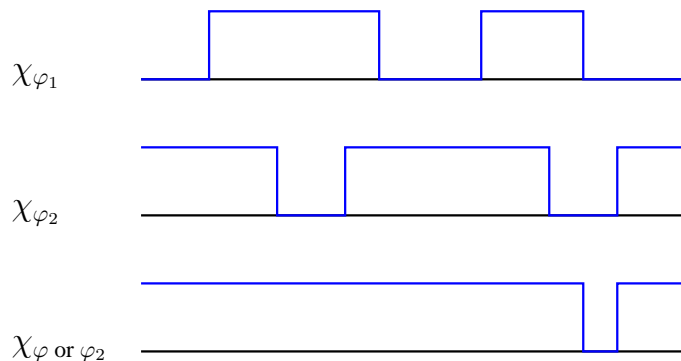
- ◆ For every positive interval  $I \in \chi_{\phi_1}$
- ◆ Compute its **back shifting**  $I - [a, b] \cap \mathbb{T}$
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# COMBINE: *Disjunction and Eventually*

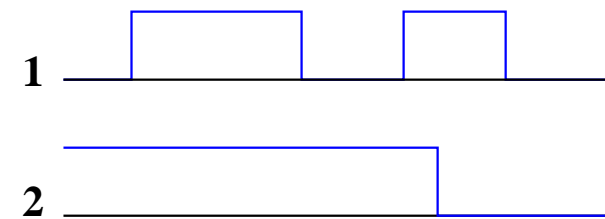
## ● Disjunction

- ❖ Refine the intervals of  $\chi_{\phi_1}$  and  $\chi_{\phi_2}$  so that the mutual values of both signals become uniform in every interval
- ❖ Compute the disjunction interval-wise
- ❖ Merge the adjacent intervals having the same value



## ● Bounded Eventually

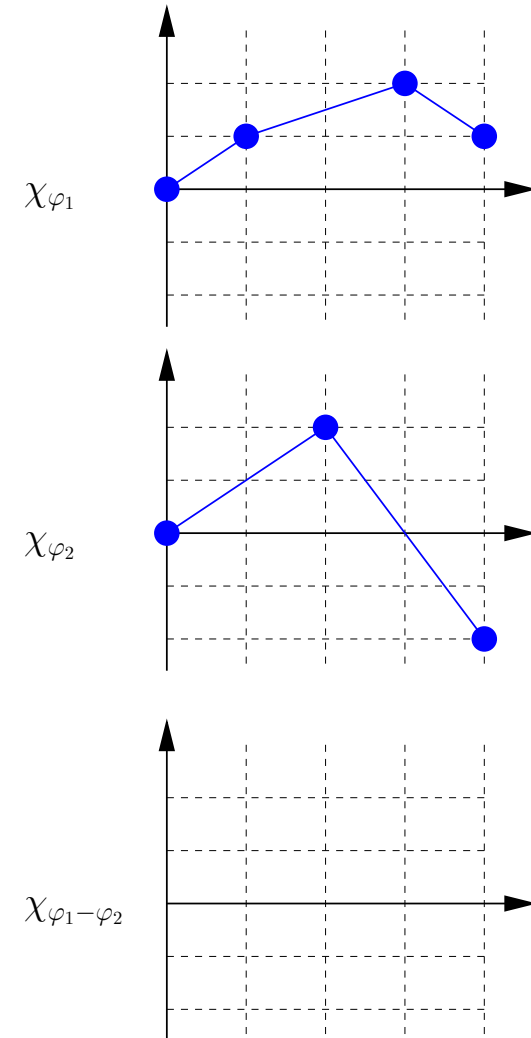
- ❖ For every positive interval  $I \in \chi_{\phi_1}$
- ❖ Compute its **back shifting**  $I - [a, b] \cap \mathbb{T}$
- ❖ Merge the overlapping intervals in  $\chi_{\phi}$



1 -  $\chi_{\phi_1}$   
2 - **eventually!** $[a, b] \chi_{\phi_1}$

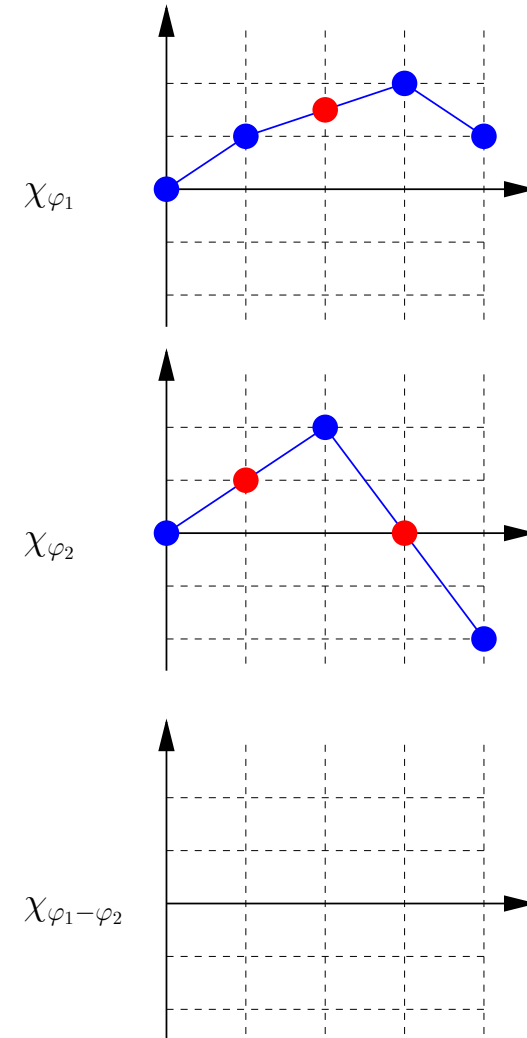
## COMBINE: *Arithmetic Operations*

- Pointwise arithmetic operation on two signals
- Take the union of their sampling points
- Extend each signal to the new points by interpolation
- Apply the operation on each pair of sampling points



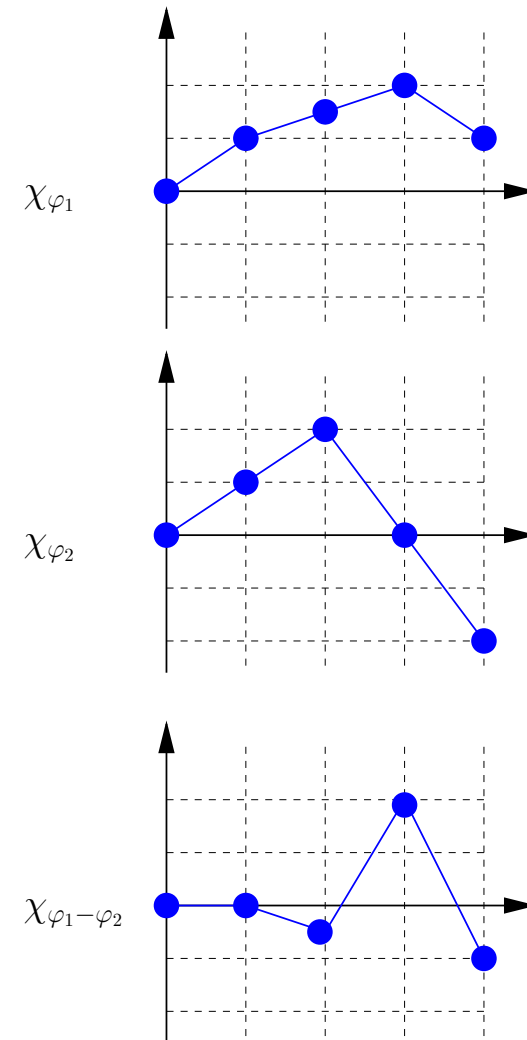
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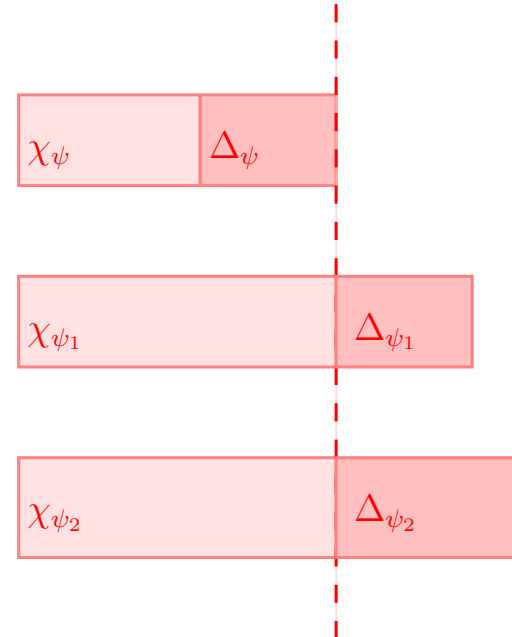
# Incremental Marking

---

---

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input : STL/PSL Temporal Formula  $\varphi$  and increment  $\Delta_\xi$ 
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switch  $\varphi$  do
  case  $p$ 
    |  $\Delta_\varphi := \Delta_\varphi \cdot \pi_p(\Delta_\xi);$ 
  end
  case  $OP_2(\varphi_1, \varphi_2)$ 
    INCREMENTAL ( $\varphi_1, \varphi_2$ );
     $\alpha_\varphi := \text{COMBINE}(OP_2, \chi_{\varphi_1}, \chi_{\varphi_2});$ 
     $d := |\alpha_\varphi|;$ 
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---





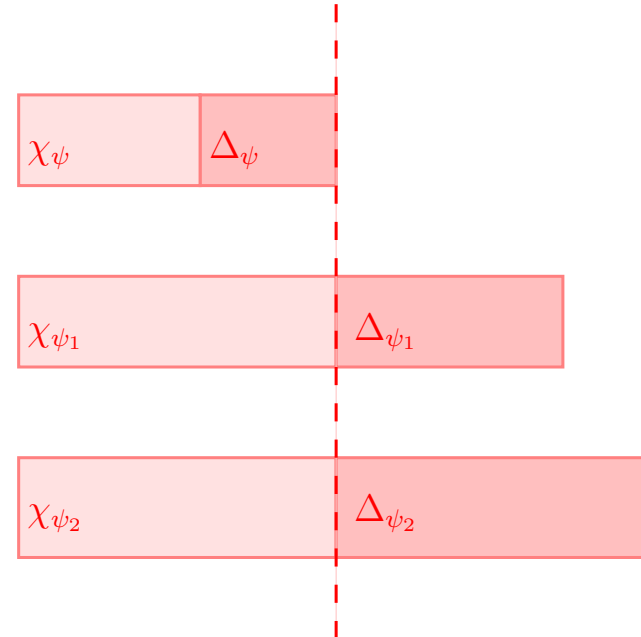
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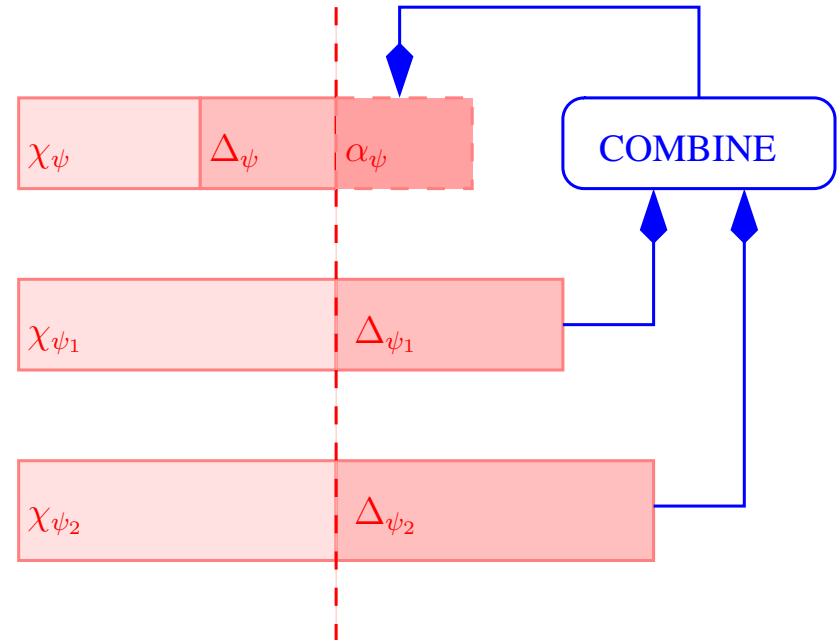
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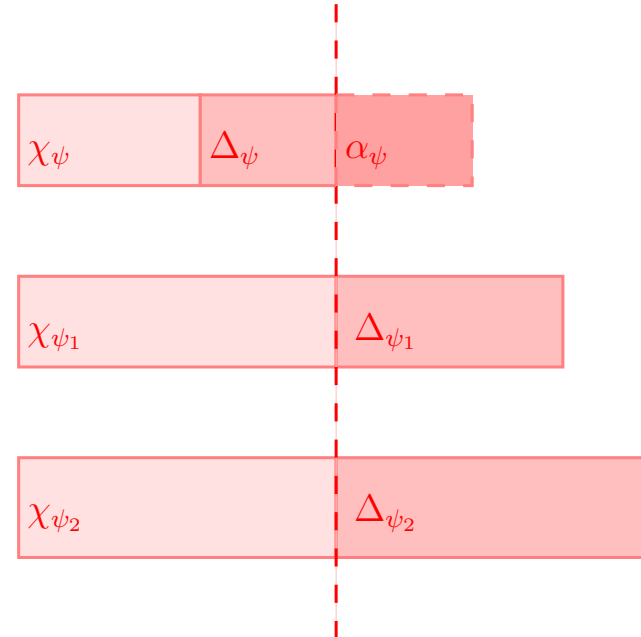
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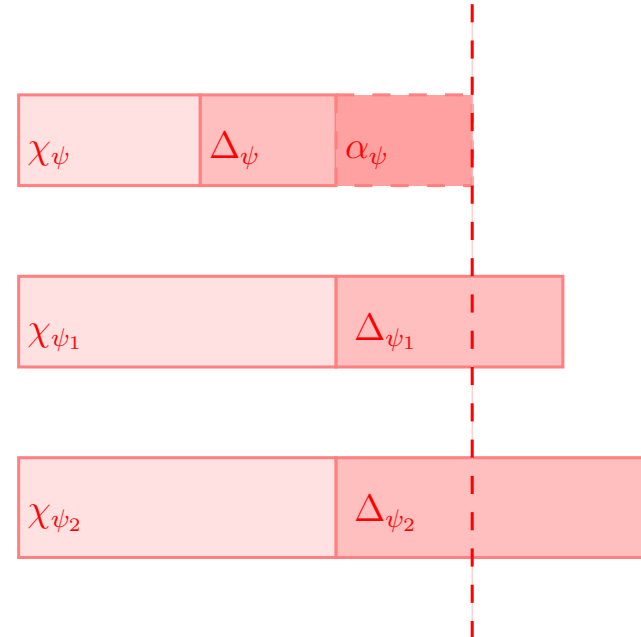
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---



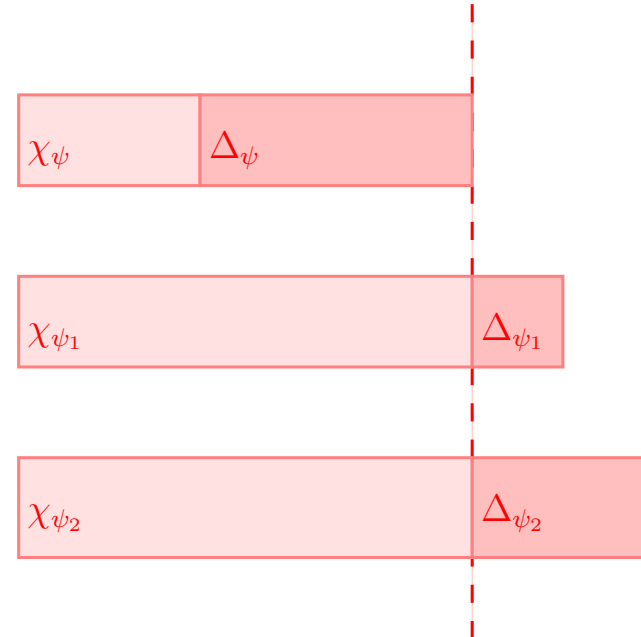
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---

---

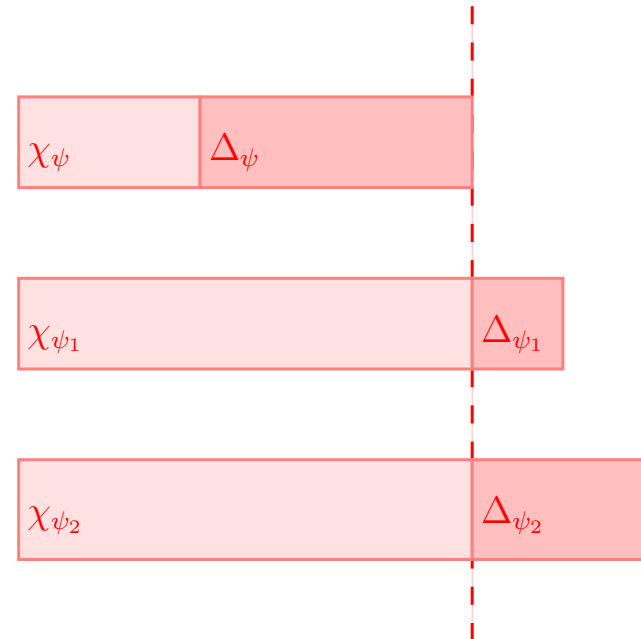
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```

---



# Incremental Marking

- Advantages of the incremental algorithm
  - ❖ Often more memory efficient
    - Determined parts of the signal may be discarded
  - ❖ Early detection of errors



# AMT *Tool Overview*

- Stand alone tool for lightweight verification of properties on continuous signals
- **Inputs:**
  - ❖ STL/PSL specification
  - ❖ Input signals (Boolean or continuous)
    - From a file (**raw**, **vcd** and **out** format)
    - Dynamic inputs through TCP/IP packets
- **Property evaluation:**
  - ❖ Offline
  - ❖ Incremental
- Visual evaluation of results

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# AMT Tool: Main Window

The screenshot displays the AMT 0.2 main window, which is divided into several functional areas:

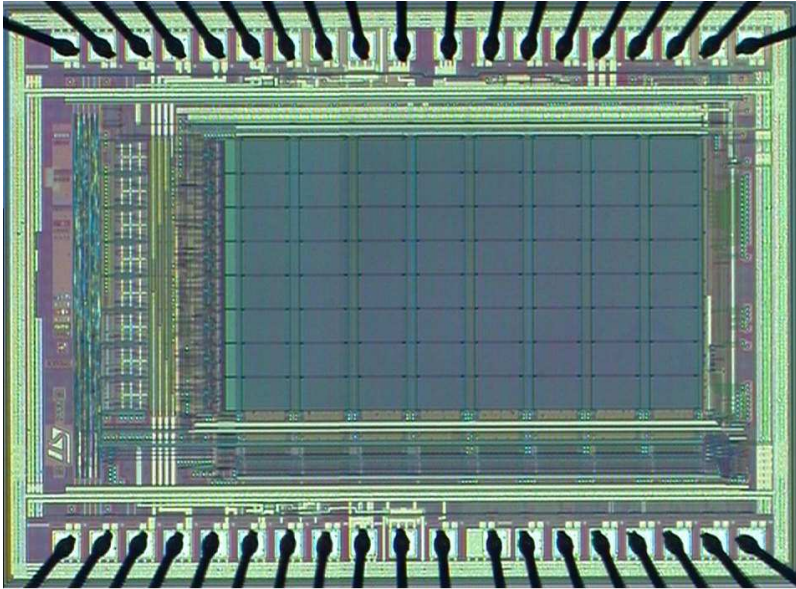
- Property Edit:** Contains Verilog-style property definitions:

```
vprop programming {  
  define b:vt_raise :=  
    a:vt <= 5.0 and eventually! [ <= 0.1 ] a:vt > 5.0;  
  define b:id_fall :=  
    abs(a:id) > 5e-6 and  
    (eventually! [ <= 0.1 ] abs(a:id) <= 5e-6);  
  
  pgm assert:  
  always (b:vt_raise ->  
    (((abs(a:id) > 5e-6) and (a:vt > 4.5))  
    until! b:id_fall));
```
- Property List:** A table listing properties:

	Name
0	programming
1	pwell
2	erasing_mode
- Property Structure View:** A tree view showing the hierarchical structure of the 'programming' property, including nodes for 'B', 'eventually!', 'pgm', 'always', 'B', 'define', and 'vt\_raise'.
- Signal List:** A table listing signals:

	Name
1	pw
2	s
3	bl
4	vt
5	id
- Signal Plots:** Five vertically stacked plots showing signal waveforms over time (0 to 5000).
  - Plot 1: **always ((vt\_raise -> (((abs(id) > 5e-06) and (vt > 4.5))) until! (id\_fall)))**. Shows a constant high signal (1) until approximately time 4800.
  - Plot 2: **vt\_raise**. Shows a high signal (1) until approximately time 2500, then drops to 0.
  - Plot 3: **(((abs(id) > 5e-06) and (vt > 4.5))) until! (id\_fall)**. Shows a high signal (1) until approximately time 3200, then drops to 0.
  - Plot 4: **id\_fall**. Shows a high signal (1) at approximately time 500 and time 3200, otherwise 0.
  - Plot 5: **abs(id)**. Shows a red curve representing the absolute value of the 'id' signal. A horizontal blue line indicates a **Threshold = 5e-06**.

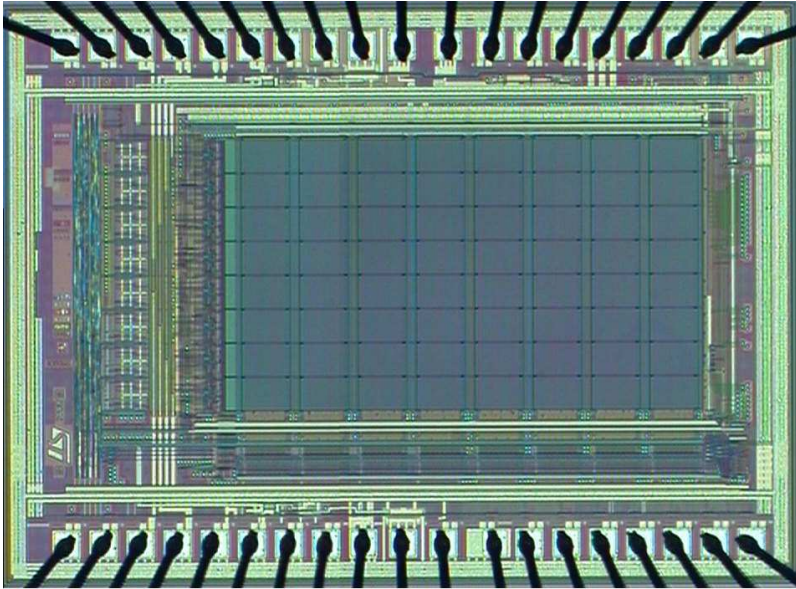
# FLASH *Memory Case Study*



- Provided by STM Italy
- Why Flash memory?
  - ❖ **Analog** circuit that implements **digital** behavior
  - ❖ Good connection between **analog** and **digital** worlds

- Different modes
  - ❖ Programming, reading, erasing, etc.
- Characteristic signals
  - ❖ **bl**: bit line terminal
  - ❖ **pw**: p-well terminal
  - ❖ **wl**: word line
  - ❖ **s**: source terminal
  - ❖ **vt**: threshold voltage of cell
  - ❖ **id**: drain current of cell
- Correct functioning in a given mode determined by the behavior of the characteristic signals
- 5 properties specifying the correct behavior

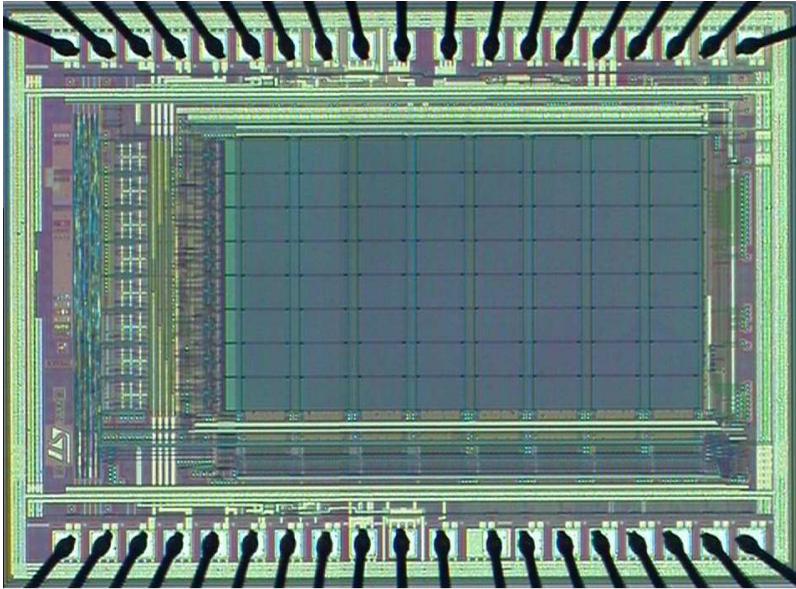
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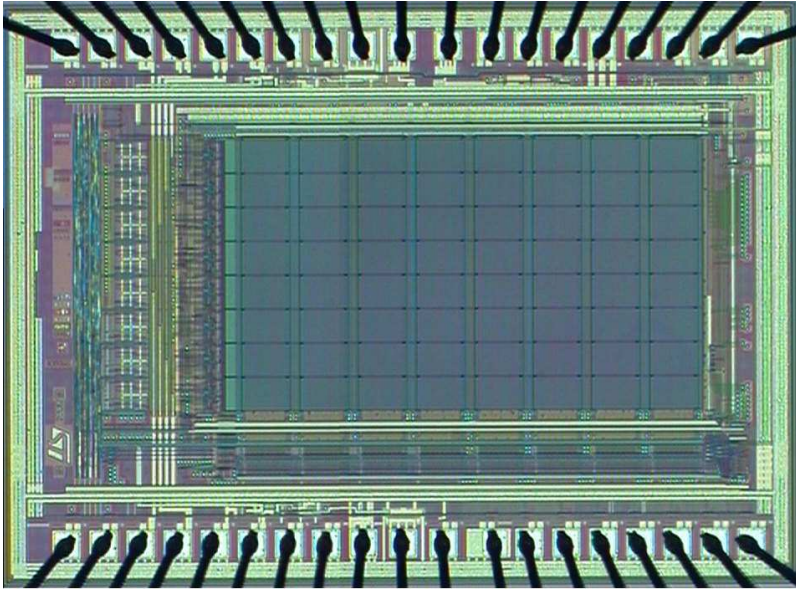


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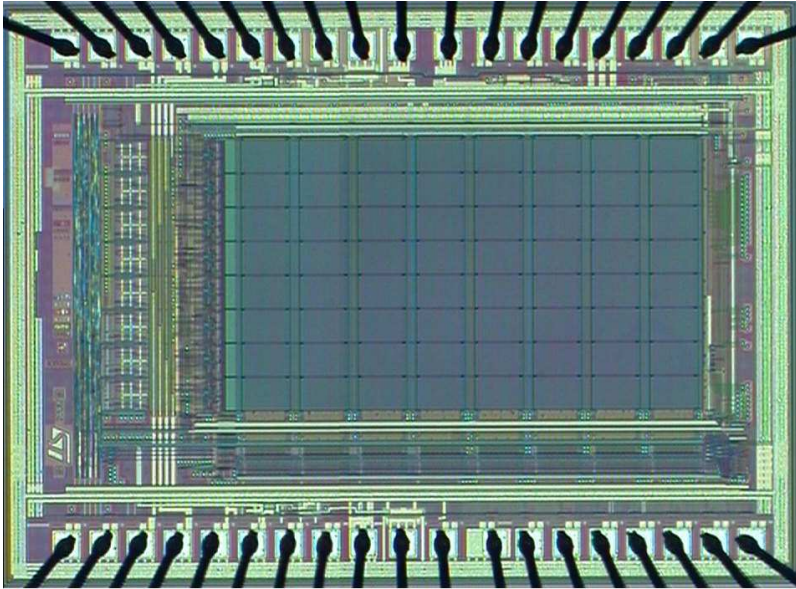
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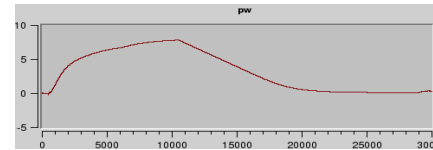
# Case Study Example: Erasing Property

```

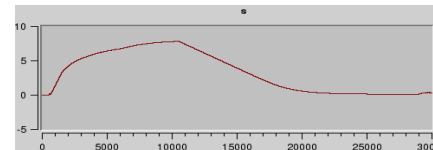
vprop erasing {
  define b:erasing_cond :=
    a:w1 <= -6 and a:pw > 5;

  erasing assert:
    always (b:erasing_cond ->
      (distance (a:s,a:pw,0.1)
        and (a:bl-a:pw)>-0.83));
}

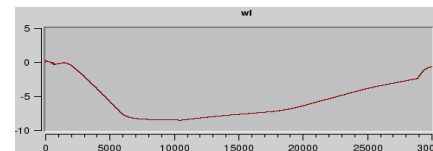
```



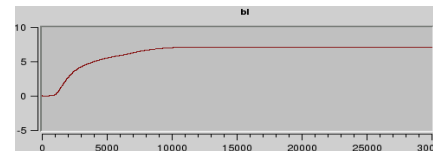
(a)



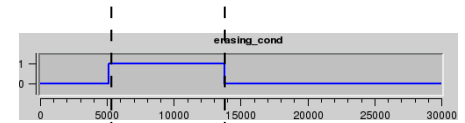
(b)



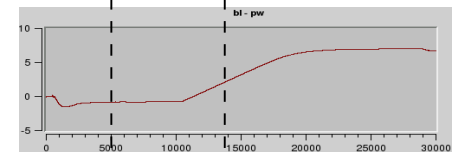
(c)



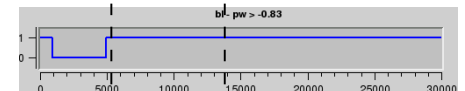
(d)



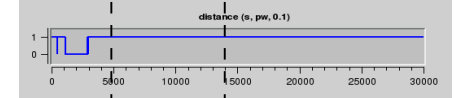
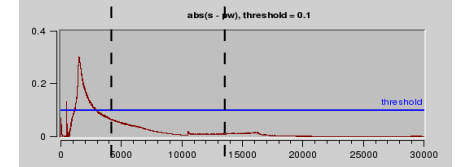
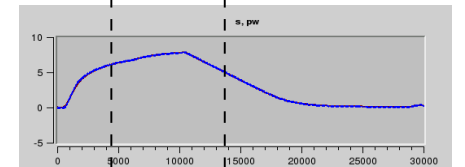
(e)



(f)



(g)



(h)

# Tool Evaluation

<b>name</b>	<b>pgm sim # intervals</b>	<b>erase sim # intervals</b>
<b>wl</b>	34829	283624
<b>pw</b>	25478	283037
<b>s</b>	33433	282507
<b>bl</b>	32471	139511
<b>id</b>	375	n/a

Table 1: Input Size

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Table 1: Input Size

<b>property</b>	<b>time (s)</b>	<b># intervals</b>
<b>programming1</b>	0.14	99715
<b>programming2</b>	0.42	405907
<b>p-well</b>	0.12	89071
<b>decay</b>	0.50	594709
<b>erasing</b>	2.35	2968578

Table 2: Offline Algorithm Evaluation

# Tool Evaluation

name	pgm sim # intervals	erase sim # intervals
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decay	0.50	594709
erasing	2.35	2968578

Table 2: Offline Algorithm Evaluation

Property	Offline t = total # intervals	Incremental m = max # active intervals	m/t * 100
programming1	99715	65700	65.9
programming2	594709	242528	40.8
p-well	89071	8	0.01
decay	594709	279782	47.1

Table 3: Offline/Incremental Space Requirement Comparison

# Conclusion

- **Main contributions:**
  - ❖ AMT tool that monitors temporal properties of continuous signals
    - Description of properties in STL/PSL specification language
    - Offline and incremental algorithms
    - Integration with numerical simulators via simulation dump files or TCP/IP link
  - ❖ FLASH memory case study
    - Validates the tool and the approach
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