Open Questions for the Bus-Blocking Problem in the 3-Phase Task Model under Partitioned Scheduling

Presentation 1 - Junior Presentations

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Outline

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Motivation: Shared resources bring timing unpredictability

Computing Power

Energy Efficiency

Inter-core Interference

Soft Real-Time Systems

Hard Real-Time Systems
Introduction: Phased Execution Model can Reduce Shared Resource Contention
3-Phase Task Model

\[
\tau_1 \in x \\
\tau_2 \in y
\]

Diagram showing the 3-Phase Task Model with interactions between System Bus, Local Memory, and Main Memory.
Problem Definition: Bus Blocking in 3-phase Task Model

Dependent on:
- Number of memory phases
- Size of memory phases
- Task priorities
- Bus arbitration Policy
Maia et al. (RTCSA 2017) [1] proposed the bus-contention aware WCRT analysis for the 3-phase task model using fixed-priority global scheduling.


Arora et al. (RTNS 2021) [3] proposed a bus-contention aware WCRT analysis for fixed-priority 3-phase task model using partitioned scheduling.
Open Issues

- The work of Maia et al. (RTCSA 2017) [1] does not focus on partitioned scheduling.

- The work of Casini et al. (RTAS 2018) [2] assumes an architecture that makes use of crossbar switch for point-to-point communication between each core and main memory. Thus, their analysis may not be applicable to architectures that makes use of shared bus.

- The work of Arora et al. (RTNS 2021) [3] focus on bus blocking problem in partitioned scheduling but it has following limitations:
  - The bus-blocking analysis is limited to FCFS bus arbitration.
  - The bus-blocking analysis is based on an assumption that if there is an pending A-phase that is to be executed on a given core, it can execute immediately after the completion of a R-phase without releasing the bus (i.e., back-to-back execution of R and A-phases on the same core).

  Such assumptions limits the applicability of the analysis.
  - Not applicable to systems that cannot comply with the assumption back-to-back execution of R and A-phases.
  - Not applicable to systems that use other bus arbitration policies.
Possible Solution

Bus Arbitration Policy
- FCFS
- Round-Robin
- TDMA
- Fixed-Processor Priority
- Fixed-Task Priority

General Framework for Bus-Contention Analysis for the 3-Phase Task Model using Partitioned Scheduling

Bus-Contention Aware Schedulability Analysis

Generic Solution
- Should not need any special provisions such as back to execution of R and A-phase in order to be applicable for any system that makes use of 3-phase task model.
Ongoing work

- We have formulated the bus-contention analysis for FCFS bus arbitration. Unlike the existing work, we do not enforce the assumption of back-to-back execution of R and A-phases.

- We are currently working on the bus-contention analysis for round-robin bus arbitration and analyzing the impact of slot size on the bus-contention and schedulability analysis.

- Furthermore, we are also working on the bus-contention analysis for processor-priority bus arbitration by assuming the global memory preemptions, a concept that was introduced by Schwäricke (ECRTS 2020) [4].
We also identified the issues that may arise when the bus-arbitration policy is fixed-task priority. For instance, what can happen if the highest-priority task and lowest-priority task are mapped on the same core.
Conclusion

- In this work, we discuss the problem of bus-blocking in the 3-phase task model under partitioned scheduling.
- We identified the open issues that have not been addressed in the state-of-the-art.
- Finally, we highlighted the possible directions and ongoing work to address the open issues.


Thank You!