Mapping and Scheduling Streaming Applications using SMT Solvers

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Multi-core Processors Everywhere



Multi-core Processors Everywhere





Multi-core Processors Everywhere





Multi-core systems



How To:



Multi-core systems



How To:

• Deploy the application to the platform



Multi-core systems



How To:

- Deploy the application to the platform
- Decide number of processors to use?



Multi-core systems



How To:

- Deploy the application to the platform
- Decide number of processors to use?
- Allocate tasks to processors and schedule them

























Application Model

Task Graph





Application Model

Task Graph



• Tasks : Software procedure



Application Model

Task Graph



• Tasks : Software procedure

annotated with execution time



Application Model

Task Graph



- Tasks : Software procedure
- Edges : Precedence relations



Deployment Problem



- Tasks : Software procedure
- Edges : Precedence relations

Deployment Problem

Task Graph

Deployment Solution





- Tasks : Software procedure
- Edges : Precedence relations

● Mapping : Task ⇒ Processor



Deployment Problem

Task Graph

Deployment Solution





- Tasks : Software procedure
- Edges : Precedence relations

- Mapping : Task ⇒ Processor
- Scheduling : Task \Rightarrow Time



Deployment Problem





Deployment Problem







Solution space is large

ıΒ 10 . 6 6 2 proc., 10 tasks \approx 1000+ potential solutions . 6 6



Deployment problem

How to:

• find optimal solutions in exponential design space.



Deployment problem

How to:

- find optimal solutions in exponential design space.
- model complex hardware which has Processors, Network, DMA



Deployment problem

How to:

- find optimal solutions in exponential design space.
- model complex hardware which has Processors, Network, DMA
- evaluate multiple criteria
 - Latency
 - Memory used
 - Processors used
 - ...



Outline





- Opployment using SMT
- Symmetry elimination
- Distributed memory scheduling
- 6 SMT Solving

Conclusions



Overview

Motivation

- 2 Application Model
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Model of Computation

Synchronous Dataflow graphs (SDF)

by Edward Lee and David Messerschmitt in 1987



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Synchronous DataFlow





Synchronous DataFlow







Synchronous DataFlow



Actors





Synchronous DataFlow



- Actors
- Edges




Synchronous DataFlow



- Actors
- Edges
- Rates





Synchronous DataFlow



Task Graph



Synchronous DataFlow



- Actor Blur is compact representation of data parallel tasks.
- All Blur tasks have **same properties** such as execution time.

Task Graph



Split-Join Graphs

we use split-join graphs : restriction of SDF

still covering perhaps 90% of use cases in the literature



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a simple example:



- α : spawn and split
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Restrictions compared to general SDF

Split-join does not support:

Stateful actors





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Split-join does not support:

- Stateful actors
- Non-proportional rates





Restrictions compared to general SDF

Split-join does not support:

- Stateful actors
- Non-proportional rates
- Initial tokens and cyclic paths





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- Boolean variables
 - in₀, in₁, in₂ ...
 - out_0 , out_1 , out_2 ...





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 - $\operatorname{out}_0 = \operatorname{in}_0 \lor \operatorname{in}_1 \oplus \operatorname{in}_2 \dots$





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SMT extends SAT by numeric variables and constants







| Actor | Α | В | | | | С |
|-------------|----------------|-------|-------|-------|-----------------------|----------------|
| Tasks | A ₀ | B_0 | B_1 | B_2 | B ₃ | C ₀ |
| Description | Variables | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |





| Actor | A B | | | | С | |
|-------------|-----------------|--------|--------|--------|-----------------------|-----------------------|
| Tasks | A ₀ | B_0 | B_1 | B_2 | B ₃ | C ₀ |
| Description | Variables | | | | | |
| Start time | xA ₀ | xB_0 | xB_1 | xB_2 | xB ₃ | xC_0 |
| | | | | | | |
| | | | | | | |





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| Description | Variables | | | | | |
| Start time | xA ₀ | xB ₀ | xB_1 | xB_2 | xB_3 | xC_0 |
| Allocated proc. | pA_0 | pB ₀ | pB_1 | pB_2 | pB_3 | pC_0 |
| | | | | | | |





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- Precedence Constraints
 - $xB_0 \ge (xA_0 + dA)$





Encoding deployment with constraints



В С Actor Α Tasks C_0 A_0 B_0 B_1 B₂ B_3 Description Variables Start time xA_0 xB₀ xB₁ xB₂ xB_3 xC_0 Allocated proc. $\mathbf{p}\mathbf{B}_1$ pB_2 pC_0 pA_0 pB_0 pB_3 Duration dA dB dC

lask Graph





Encoding deployment with constraints



| Actor | A B | | | | С | |
|-----------------|-----------------|--------|--------|--------|-----------------------|-----------------------|
| Tasks | A ₀ | B_0 | B_1 | B_2 | B ₃ | C ₀ |
| Description | Variables | | | | | |
| Start time | xA_0 | xB_0 | xB_1 | xB_2 | xB_3 | xC_0 |
| Allocated proc. | pA ₀ | pB_0 | pB_1 | pB_2 | pB ₃ | pC ₀ |
| Duration | dA | dB | | | | dC |

- Precedence Constraints
 - $xB_0 \ge (xA_0 + dA)$
- Mutual Exclusion Constraints

$$\bullet \mbox{ if } (pB_1=pB_2) \mbox{ then } \\ xB_1 \geq (xB_2+dB) \ \lor \ xB_2 \geq (xB_1+dE)$$

Latency Cost

• Latency = $(\mathbf{x}\mathbf{C}_0 + \mathbf{d}\mathbf{C})$





Multi-criteria Problem





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Multi-criteria Problem



Multi-criteria Problem



Multi-criteria Problem



















Problem Monotonicity

Latency = 4 #Proc = 2 Not Possible





Problem Monotonicity

Latency = 4 #Proc = 2 Not Possible Latency = 2 #Proc = 1 Also Not Possible




Problem Monotonicity

Latency = 4 #Proc = 2 Not Possible Latency = 2 #Proc = 1 Also Not Possible





Design Space Exploration

Split-join Graph



























Design Space Exploration



Timeout: Cannot decide SAT / UNSAT in a given TIME-BUDGET.









• Divide cost space using grids





- Divide cost space using grids
- One SMT query per point on the grid





- Divide cost space using grids
- One SMT query per point on the grid
- Finer grid after every iteration



• sat points • not yet explored points



- Divide cost space using grids
- One SMT query per point on the grid
- Finer grid after every iteration
- Don't query in known area





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- all instances of actor C are similar (symmetric)
- No change in latency !





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- Huge number of such symmetric solutions





- all instances of actor C are similar (symmetric)
- No change in latency !
- Huge number of such symmetric solutions
- Add constraints to eliminate all but one









• lexicographic order : $C_{00} \ll C_{01} \ll C_{10} \ll C_{11}$





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- enforce lexicographic order in schedule: s(u) < s(u') for $u \ll u'$





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Task Symmetry : Theorem



• Theorem : Every group has a lexicographic schedule





- Theorem : Every group has a lexicographic schedule
- Corollary : No feasible cost is lost



Processor Symmetry





Processor Symmetry



Processor Symmetry


Pareto Exploration

Exploration : Processors vs Latency $\alpha = 30$



Pareto Exploration



without symmetry breaking



Exploration : Processors vs Latency $\alpha = 30$



Pareto Exploration



Exploration : Processors vs Latency $\alpha = 30$



Pareto Exploration



3D cost space $(\mathbf{C}_L, \mathbf{C}_P, \mathbf{C}_B)$ exploration, \mathbf{C}_B - total buffer size

MPEG video decoder:





3D cost space $(\mathbf{C}_L, \mathbf{C}_P, \mathbf{C}_B)$ exploration, \mathbf{C}_B - total buffer size

MPEG video decoder: 20 150 1 1500 20 1 100 1/20 3400 5 4 300 1 200 1/4 30 40 1 4 122 Tasks





3D cost space $(\mathbf{C}_L, \mathbf{C}_P, \mathbf{C}_B)$ exploration, \mathbf{C}_B - total buffer size

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Better Pareto points

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3D cost space $(\mathbf{C}_L, \mathbf{C}_P, \mathbf{C}_B)$ exploration, \mathbf{C}_B - total buffer size





Distributed memory scheduling

• So far we ignored the communication costs



Distributed memory scheduling

- So far we ignored the communication costs
- For distributed memory, communication needs to be modeled



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Kalray MPPA-256

| 512 KB | USMC | | PCle | inter laken | | DDR |
|----------------|------|------|------|-------------|--|--------------|
| Quad Core | | | | | | GPIOs |
| E. | | | | | | _ |
| Inter Iaken | | | | | | Inter |
| Quad Core | | | | | | Quad |
| 512 KB | | | | | | KB 512 |
| DDR | | | | | | Quad Core |
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Kalray MPPA-256



• 16 compute clusters



Kalray MPPA-256



• 16 compute clusters



Kalray MPPA-256



16 compute clusters
16 processors



Kalray MPPA-256



- 16 compute clusters
 - 16 processors
 - 2 MB Shared Memory



Kalray MPPA-256



• 16 compute clusters

- 16 processors
- 2 MB Shared Memory
- DMA



Kalray MPPA-256



• 16 compute clusters

- 16 processors
- 2 MB Shared Memory
- DMA
- Toroidal 2D network



The problem?

- Which cluster to allocate?
- Which processor to allocate?
- Connected tasks in same or different cluster?
- Communicating tasks if to be added, which DMA?
- And the constraints
 - Precedence
 - Mutual Exclusion
 - Costs

For 10 tasks, 256 processors, $1.20892582 imes 10^{24}$ potential solutions!



The problem?

- Which cluster to allocate?
- Which processor to allocate?
- Connected tasks in same or different cluster?
- Communicating tasks if to be added, which DMA? Split the problem into sub-problems.
- And the constraints
 - Precedence
 - Mutual Exclusion
 - Costs

For 10 tasks, 256 processors, $1.20892582 imes 10^{24}$ potential solutions!



Design Flow

Application Graph



Design Flow





Design Flow



Goals

- Load balance the groups
- Minimize data exchange



Design Flow





Design Flow



Goals

Minimize distance between communicating groups

Design Flow





Design Flow



Goals

- Minimize Latency
- Minimize Buffer size



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Tasks and Transfers



- Tasks and Transfers
 - Cluster Mapping



- Tasks and Transfers
 - Cluster Mapping
 - Processor and DMA Mapping



- Tasks and Transfers
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 - Processor and DMA Mapping
 - Start time



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- Tasks and Transfers
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- Application
 - Latency



DMA Model

Tasks communicating via DMA:





DMA Model

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DMA Model

Tasks communicating via DMA:



| Task Description | | Resources used | Task duration | |
|------------------|----------------|-------------------|---------------|--|
| I | Initialization | Processor and DMA | Constant | |



DMA Model

Tasks communicating via DMA:





| Task | Description | Resources used | Task duration | |
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| G | Network Transfer | Only DMA | Transfer size dependent | |



Model Transformation

An example application graph:





Model Transformation

An example application graph:





Model Transformation

An example application graph:



Partition-Aware graph:





Model Transformation

An example application graph:



Partition-Aware graph:





Model Transformation

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Model Transformation

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Partition-Aware graph:







Model Transformation

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Partition-Aware graph:







JPEG Decoder Example





JPEG Decoder Example



VLD : Variable Length Decoder



JPEG Decoder Example



VLD : Variable Length Decoder

IQ / IDCT : Inverse Quantization / Inverse Discrete Cosine Transform



JPEG Decoder Example



VLD : Variable Length Decoder

IQ / IDCT : Inverse Quantization / Inverse Discrete Cosine Transform

Color : Color Conversion





- C_z : No. of Groups
- C_{η} : Total communication cost
- $C_{ au}$: Max. workload per group





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| Solution | Allocated group | | | Exploration Cost | | |
|----------|-----------------|----|-------|---------------------------|---------------------|--------------------|
| Solution | vld | iq | color | $\mathbf{C}_{\mathbf{z}}$ | \mathbf{C}_{η} | $\mathrm{C}_{	au}$ |
| P_{s0} | 0 | 1 | 2 | 3 | 12384 | 424012 |
| P_{s1} | 0 | 0 | 1 | 2 | 2736 | 758116 |
| P_{s2} | 0 | 0 | 0 | 1 | 0 | 934288 |
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JPEG Decoder Example



JPEG decoder latency measured on Kalray platform



- e- model ---- measured-min. ---- measured-max.



JPEG decoder latency measured on Kalray platform



- - model ---- measured-min. ---- measured-max.

Maximum prediction error of 9%

StreamIt Benchmarks



StreamIt Benchmarks



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Lessons learnt from SMT solver





Lessons learnt from SMT solver



Such constraints makes the problem **harder** for SMT



Two-step optimization

• Get a loose schedule from the solver





Two-step optimization

- Get a loose schedule from the solver
- **Optimize** it for:
 - Latency
 - Processors used





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Conclusions and Future Work

Conclusions:

• Symmetry elimination finds better solutions



Conclusions and Future Work

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- Symmetry elimination finds better solutions
- Combined Optimization with Communication modeling



Conclusions and Future Work

Conclusions:

- Symmetry elimination finds better solutions
- Combined Optimization with Communication modeling
- Automated design flow for distributed memory



References

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Thank You



Questions?

