

CURRICULUM VITAE

Stavros Tripakis

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RESEARCH INTERESTS

Modeling, analysis and implementation of embedded systems. Component-based design. Verification and synthesis. Testing and fault diagnosis. Concurrent, distributed and multicore systems.

EMPLOYMENT

- 03/2010 – present: Associate Research Engineer, University of California, Berkeley, USA.
- 02/2009 – 02/2010: Visiting Associate Research Engineer, University of California, Berkeley, USA.
- 02/2006 – 11/2008: Research Scientist, Cadence Research Laboratories, Cadence Design Systems, Inc., Berkeley, CA, USA.
- 04/2001 – 02/2006: Research Scientist (“Chargé de Recherche”), CNRS (“Centre National de la Recherche Scientifique”), Verimag Laboratory, France. (On leave since 02/2006.)
- 04/2000 – 03/2001: Visiting Assistant Research Engineer, California PATH (Partners for Automated Transit and Highways), Caltrans and University of California, Berkeley, USA.
- 02/1999 – 03/2000: Visiting Scholar, Electronics Research Laboratory, University of California, Berkeley, USA.
- 09/1990 – 12/1993: Research Assistant at the Computer Science Institute, Foundation of Research and Technology, Hellas, Heraklion, Greece.

EDUCATION

- 10/1995 – 12/1998: Ph.D. in Computer Science, Joseph Fourier University, Grenoble, France.
Dissertation: *The formal analysis of timed systems in practice.*

- 10/1994 – 07/1995: M.Sc. in Computer Science and Mathematics, École Normale Supérieure of Paris, École Polytechnique, Universities of Paris VI, VII and XI.
 - 10/1988 – 12/1993: Bachelor degree and postgraduate studies in Computer Science and Mathematics, University of Crete at Heraklion, Greece.
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CONSULTANCIES

- 10/2004 – 12/2004: Consultant for RATP (the Paris subway operator), France.
 - 09/2000 – 01/2001: Consultant for Terablaze Inc., Cupertino, CA, USA.
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AWARDS AND HONORS

- Paper [16] was voted *Best Paper*.
 - Paper [20] received the *ACM SIGSOFT Distinguished Paper Award*.
 - “Jury compliments” (“Félicitations du jury”) for my Ph.D. thesis. Given to less than 5% of theses defended at Joseph Fourier University.
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RESEARCH GRANTS AND PROJECTS

Funded proposals at UC Berkeley:

- Proposal *CPS: Medium: Timing-Centric Software*, funded by NSF Cyber Physical Systems Program, 9/15/10 - 8/31/13. Co-author and Investigator. 750 K USD for 3 years.

Proposals submitted and pending:

- *Expeditions in Computer Augmented Program Engineering (ExCAPE) – Harnessing Synthesis for Software Design*, submitted to NSF Expeditions in Computing Program, 09/2010. Co-author and Investigator.

At UC Berkeley, participating in:

- The Center for Hybrid and Embedded Software Systems ([CHESS](#)).
- The Multiscale Systems Center ([MuSyC](#)).

Primary industrial collaborations within CHESS:

- With Thales Research and Technology, France, on integrating Berkeley’s modeling tool Ptolemy and Thales’ parallel application mapping tool Spear-DE.
- With Bosch Research and Technology Center North America, on static checking consistency of automotive industrial models.
- With National Instruments, on system-level and interface-based design.

Proposals funded while at Verimag, France (2001 – 2006):

- 1/2002–2/2004: European IST project *NEXT TTA – High-Confidence Architecture for Distributed Control Applications*. Verimag PI. 400 K EUR.
- 9/2003–9/2006: Research grant recipient by the Rhône-Alpes region on *Design and implementation of embedded software components*. 90 K EUR.
- 9/2004–9/2005: Research contract with RATP (the Paris subway operator) on the verification of a subway signaling station. Co-PI. 60 K EUR.
- 7/2004–6/2005: Recipient of a “young researcher” grant by CNRS. 26 K EUR.
- 9/2003–9/2006: French project *CORTOS – Control and Observation of Real-Time Open Systems*. Verimag PI. 25 K EUR.
- 10/2001–03/2003: French project *eKronos – Timing analysis of embedded software*. Co-PI. 20 K EUR.
- 1/2005–12/2005: French project *Emtest – Testing of embedded systems*. Co-PI. 13 K EUR.
- 9/2003–9/2004: France-Berkeley Fund project *Service Networks – Intelligent middleware for distributed applications*. Co-PI. 10 K USD.

Participation in other projects at Verimag:

- 8/2002–2/2005: European IST project *RISE – Reliable Innovative Software for Embedded Systems*. Verimag co-PI.
- Member of the *Artist Network of Excellence on Embedded Systems* (2001 – 2006). Verimag PI for the *Testing and Verification Cluster* and the *Distributed and Real-Time Observation and Control Activity*.

Participation in other projects at UC Berkeley (during post-doc, 1999 – 2001):

- DARPA projects *MoBIES – Model Based Integration of Embedded Systems and Smart Networks*, and in ONR project *Distributed Autonomous Agent Networks*.

STUDENTS AND POSTDOCS

Advisor of graduated Ph.D. students:

- Adrian Curic, 10/2001 – 10/2005, *Distributed Code Generation from Lustre Programs*. Co-advised with Dr. Paul Caspi.
- Christos Sofronis, 10/2002 – 11/2006, *Embedded Code Generation from High-Level Heterogeneous Components*. Co-advised with Dr. Paul Caspi.
- Moez Krichen, 10/2003 – 12/2007, *Model-Based Testing for Real-Time Systems*.
- Nazha Abed, 10/2005 – 07/2009, *Randomized Exploration of Large State Spaces for Verification*. Co-advised with Prof. Jean-Marc Vincent.

Mentor of:

- At UC Berkeley: Ph.D. students: Chris Shaver (since Apr'10), Dai Bui (since Feb'09), Ben Lickly (since Feb'09), Eleftherios Matsikoudis (since Jun'09), John Musacchio ('00-'01), Linhai He ('00-'01), Oleg Botchkarev ('99-'01). Master's students: Rahul Jain ('00-'01), Duke Lee ('99-'01). Undergraduates: Marco Zennaro ('00-'01), Jeff Ko ('00-'01).
- At Verimag: Postdocs: Norman Scaife ('03-'04), Aude Maignan ('01-'03). Master's students: Gérald Roudil ('03-'05), Moez Krichen ('03-'04), Mohamed Bekhieh ('03-'04), Christos Sofronis ('02-'03), Karine Altisen ('97-'98), Gregor Goessler ('97-'98). Undergraduates: Cyril Guironnet (Spring'05), Rachid Mokhtari (Spring'05), Nguyen Quang-Trung (Spring'05), Mohamed Dergueche (Spring'05), Emile Verdurae (Spring'04), Jamel Hajji (Spring'04), Maher Sebai (Spring'04).
- At Cadence Labs: Roberto Lubliner (intern, summers '07 and '08), Jochen Zimmerman (intern, Mar'08 - Sep'08), Tobias Welp and Yang Yang (UC Berkeley EE 249 class project, Fall'07).

Member of the Ph.D. thesis jury of:

- Sarah Zennou, *Partial-order verification methods for timed automata*, Marseille University, France, 2004.
- Guillaume Gardey, *Verification methods for timed Petri nets*, Rennes University, France, 2005.
- Emilie Oudot, *Contributions to the incremental verification of composite timed systems*, Franche-Comté University, France, 2006.

TEACHING

- Fall 2010, Fall 2009, Fall 2007, and Fall 2006: Total of eight 1.5-hour lectures on *The Synchronous Model of Computation* and *Exploring Models of Computation with Ptolemy II* given in graduate course *EE 249 – Design of Embedded Systems: Models, Validation and Synthesis*, Electrical Engineering and Computer Sciences Department, University of California, Berkeley.
- Fall 2010: Organizer of study group on *Topics in Parallel Computing*.
- Spring 2010: Organizer of study group on *Topics in Dataflow*.
- Spring 2010 and Spring 2009: Total of three 1.5-hour lectures given in undergraduate course *EE 149 – Introduction to Embedded Systems*, Electrical Engineering and Computer Sciences Department, University of California, Berkeley.
- Fall 2009: One 1.5-hour lecture on *The Synchronous Model of Computation* given in graduate course *CE 290I – Civil Systems: Control and Information Management*, Civil And Environmental Engineering Department, University of California, Berkeley.
- Spring 2005: co-taught graduate course *Testing Methods*, Joseph Fourier University, Grenoble, France.
- Fall 1999: co-taught undergraduate course *EE 122 – Introduction to Communication Networks*, University of California, Berkeley.
- Spring 1996: taught graduate course *Formal Methods and Verification*, University of Crete, Heraklion, Greece.

PROFESSIONAL ACTIVITIES

- Program Co-Chair: *9th International Conference on Formal Modelling and Analysis of Timed Systems – FORMATS 2011*.
- Program Co-Chair: *10th International Conference on Embedded Software – EMSOFT 2010*. <http://ptolemy.eecs.berkeley.edu/conferences/10/emsoft10/>.
- Co-organizer and speaker at the *Tutorial: Exploring Models of Computation with Ptolemy II*, Embedded Systems Week 2010. <http://ptolemy.eecs.berkeley.edu/conferences/10/tutorial/>.
- Nominated and elected Secretary/Treasurer of ACM SIGBED (Association for Computing Machinery – Special Interest Group on Embedded Systems), 07/2009 – 06/2011.
- Associate Editor, *Journal of Discrete Event Dynamic Systems*, 01/2010 – 12/2012.
- Member of Cadence Strategic Option Analysis and Market Segment Analysis teams, and Cadence Research Operations Committee, 10/2006 – 10/2008.
- Project Evaluator for European Framework Program 7, Objective: *Embedded Systems Design*, 4-7 June 2007.
- Project Reviewer of European IST project *COLUMBUS – Design of Embedded Controllers for Safety Critical Systems*, 07/2002 – 06/2004.
- Organizing Committee Member:
 - Workshop on Control and Observation of Real-Time Open Systems (CORTOS 2006), Satellite workshop of the 17th International Conference on Concurrency Theory (CONCUR 2006).
 - 2nd International Conference on Embedded Software (EMSOFT 2002).
 - Workshop on Networked Autonomous and Semi-autonomous Vehicles, Satellite workshop of the 40th IEEE Conference on Decision and Control (CDC'01).
- Journal Reviewer: ACM TECS (Trans. Embedded Computing Systems), ACM TOPLAS (Trans. Programming Languages and Systems), ACM TOSEM (Trans. Software Engineering and Methodology), Acta Informatica, Automatica, Discrete Event Dynamic Systems, EURASIP Journal on Embedded Systems, Formal Aspects of Computing, Formal Methods in System Design, IEEE TOC (Trans. Computing), IEEE TSE (Trans. Software Engineering), IEEE TCAD (Trans. Computer-Aided Design), IEEE TAC (Trans. Automatic Control), IEEE TRO (Trans. Robotics), IEEE Trans. Systems, Man, and Cybernetics–Part A: Systems and Humans, Information Processing Letters, Journal of Logic and Algebraic Programming, Logical Methods in Computer Science, Nordic Journal of Computing, SIAM Journal on Control and Optimization, Simulation, Software and Systems Modeling, Software: Practice and Experience, Software Tools for Technology Transfer, Theoretical Computer Science, The Journal of Signal Processing Systems, Transportation Research.

- Conference Reviewer: ACM Principles of Programming Languages (POPL). ACM Embedded Software (EMSOFT). ACM Languages, Compilers, and Tools for Embedded Systems (LCTES). ACM Symposium on Applied Computing (SAC). Computer Aided Verification (CAV). Design, Automation and Test in Europe (DATE). Design Automation Conference (DAC). IEEE Real-Time Systems Symposium (RTSS). IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS). IEEE Conference on Decision and Control (CDC). Hybrid Systems: Computation and Control (HSCC). Formal Methods in Computer-Aided Design (FMCAD). International Colloquium on Automata, Languages and Programming (ICALP). Verification, Model Checking, and Abstract Interpretation (VMCAI). Application of Concurrency to System Design (ACSD). Formal Modelling and Analysis of Timed Systems (FORMATS). Workshop on Discrete Event Systems (WODES). Formal Techniques for Networked and Distributed Systems (FORTE). Runtime Verification (RV). Euromicro Conference on Real-Time Systems (ECRTS).

TECHNICAL PROGRAM COMMITTEE MEMBER

- 9th International Conference on Formal Modelling and Analysis of Timed Systems (FORMATS 2011) – Program Co-Chair. Also PC Member of FORMATS 2009, 2008, 2007, 2005 and 2003.
- 2nd Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures (PARMA 2011).
- Workshop on the Design, Modeling and Evaluation of Cyber Physical Systems (CyPhy'11).
- Design, Automation and Test in Europe (DATE 2011), Track D: Design Methods, Tools, Algorithms and Languages, Topic D1: System Specification and Modelling. Also PC Member of DATE 2010, 2008 and 2007, Topic: Model Based Design of Embedded Systems.
- 14th International Conference on Hybrid Systems: Computation and Control (HSCC 2011). Also PC Member of HSCC 2010, 2009 and 2001.
- 31st IEEE Real-Time Systems Symposium (RTSS 2010) – Cyber-Physical Systems Track.
- 10th ACM International Conference on Embedded Software (EMSOFT 2010) – Program Co-Chair. Also PC Member of EMSOFT 2007.
- 1st Workshop on Hands-on Platforms and tools for model-based engineering of Embedded Systems (HoPES 2010).
- 1st International Workshop on Rewriting Techniques for Real-Time Systems (RTRTS 2010).
- 10th International Workshop on Discrete Event Systems (WODES 2010). Also PC Member of WODES 2008.
- 30th IEEE Real-Time Systems Symposium (RTSS 2009) – Design and Verification of Embedded Real-Time Systems Track.
- IEEE Symposium on Industrial Embedded Systems (SIES 2009).
- 21st International Conference on Computer Aided Verification (CAV 2009).

- 10th International Workshop on Verification of Infinite-State Systems (INFINITY 2008).
- 28th IFIP WG6.1 International Conference on Formal Techniques for Networked and Distributed Systems (FORTE 2008).
- DATE 2008 Workshop on Dependable Software Systems.
- 23rd Annual ACM Symposium on Applied Computing (SAC 2008), Technical Track on Embedded Systems: Applications, Solutions, and Techniques.
- 8th Workshop on Runtime Verification (RV 2008).
- 3rd intl Workshop on Systems Software Verification (SSV 2008).
- 13th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS 2007).
- 16th Euromicro Conference on Real-Time Systems (ECRTS 2004).
- 3rd International Conference on Application of Concurrency to System Design (ACSD 2003).
- Workshop on Real-Time Tools (RT-TOOLS 2002). Also PC Member of RT-TOOLS 2001.

INVITED TALKS

- *Compositionality and Modularity in Embedded System Design: Interface Theories and Interface Synthesis*, ECE Department Seminar, University of Maryland, Sep 17, 2010.
- *On Relational Interfaces*, RESS Seminar, University of California, Berkeley, Feb 2, 2010.
- *On the Compositionality of Synchronous (and Other) Models of Computation*. Dagstuhl Seminar on Synchronous Languages (SYNCHRON'09). Nov 22-27, 2009, Dagstuhl, Germany.
- *On Relational Interfaces*, EE Department Seminar, University of California, Los Angeles, Sep 25, 2009.
- *Implementation of Synchronous Programs on Asynchronous Execution Platforms: Correctness, Modularity, and Performance Analysis*. Caltech Workshop on Verification and Validation, Sep 23-24, 2009, Pasadena, CA.
- *Correct and Efficient Implementations of Synchronous Models on Asynchronous Execution Platforms*. CAV 2009 Workshop on Exploiting Concurrency Efficiently and Correctly – (EC)², Jun 26-27, 2009, Grenoble, France.
- *Model-Based Design: Semantics-Preserving Implementation of Synchronous Models*. CS Department, Iowa State University, Mar 5, 2009.
- *Implementing Synchronous Models on Distributed Execution Platforms*. CHES Seminar, University of California, Berkeley, Feb 24, 2009.
- *Modular Code Generation from Synchronous Block Diagrams: Modularity vs. Reusability vs. Code Size*. CHES Seminar, University of California, Berkeley, Feb 3, 2009.

- *Modular Code Generation from Synchronous Block Diagrams*. Department of Information Technology, Uppsala University, Dec 15, 2008.
- *Modular Code Generation from Synchronous Block Diagrams*. 3rd International Workshop on Foundations and Applications of Component-based Design (WFCD2008). ArtistDesign Workshop organized within Embedded Systems Week, Oct 19, 2008, Atlanta, GA.
- *Research Problems in Embedded Distributed Systems*, GSRC (Gigascale Systems Research Center) Workshop on Distributed Systems, Sep 22, 2008, Berkeley, CA.
- *Modular Code Generation from Synchronous Block Diagrams*. CAV'08 Workshop on Numerical Abstractions for Software Verification (NSV'08), Jul 8, 2008, Princeton, NJ.
- *Monitoring, Fault Diagnosis and Testing Real-time Systems using Analog and Digital Clocks*. Dagstuhl Seminar on Runtime Verification, Jan 4, 2007, Dagstuhl, Germany.
- *Black-box Conformance Testing for Real-Time Systems*. LIAFA Laboratory (Laboratoire d'Informatique Algorithmique: Fondements et Applications), University of Paris 7, Nov 11, 2005.
- *Testing and Fault-Diagnosis for Real-Time Systems*. Artist2 Summer School on Component & Modelling, Testing & Verification, and Statical Analysis of Embedded Systems, Oct 2, 2005, Nasslingen, Sweden.
- *Undecidable Problems in Decentralized Observation and Control*. CS Department Seminar, Université Libre de Bruxelles, May 19, 2005, Brussels, Belgium.
- *Testing Real-Time Systems*. LAAS Laboratory (Laboratoire d'Analyse et d'Architecture des Systèmes), May 4, 2004, Toulouse, France.
- *Testing Real-Time Systems*. NASA Ames Research Center, Mar 11, 2004.
- *Undecidable Problems in Decentralized Observation and Control*. Workshop on Automata, Distributed and Timed Models, LaBRI Laboratory (Laboratoire Bordelais de Recherche en Informatique), Nov 7, 2002, Bordeaux, France.
- *Fault-Diagnosis of Timed Systems*, BRICS Seminar, CS Department, Aalborg University, Aug 6, 2002.
- *Protocol Design and Verification*. Workshop on Networked Autonomous and Semi-autonomous Vehicles, IEEE Conference Decision and Control (CDC'01), Dec 3, 2001, Orlando, FL.
- *Undecidable Problems in Decentralized Observation and Control*. Workshop on Recent Advances in Discrete-Event Systems, Sep 7, 2001, Ann Arbor, MI.
- Panelist in *Hybrid System Applications: An Oxymoron?*, Panel of the Intl. Conf. on Hybrid Systems: Computation and Control, Mar 30, 2001, Rome, Italy.

SOFTWARE

I developed or contributed to the development of the following tools, most of which are publicly distributed. The web pages of the tools are accessible from <http://www-verimag.imag.fr/~tripakis/>.

- Developer of RT-Spin, an extension of the Spin model-checker for real-time.
- Developer of Minim, a minimization tool for timed automata.
- One of four developers of Kronos, a model-checker for timed automata.
- Developer of Open-Kronos, an extension of the SMI model-checker for timed automata.
- Supervised the development of the Simulink/Stateflow-to-Lustre translator by Ph.D. student Christos Sofronis and post-doc Norman Scaife.
- Supervised the development of the Simulink modular code generator by Cadence Labs intern student Roberto Lublinerman.

PATENTS

- *Method, system and computer program product for implementing external domain independent modeling framework in a system design*, with Yaron Kshai and Felice Balarin, filed on 12/28/2007, number CA7058312001.
- *Method and system for verifying electronic designs having software components*, with Ken McMillan, filed on 12/21/2007, number CA7057221001.
- *Generating modular and hierarchical execution code from untimed and timed block diagrams*, with Roberto Lublinerman, filed on 09/07/2007, number CA7056892001.

PROFESSIONAL ORGANIZATIONS

Member, ACM.

LANGUAGES

Greek, native. English, fluent. French, fluent. Finnish, basic.

CITIZENSHIP AND IMMIGRATION STATUS

Greek citizen. US permanent resident (green card).

COMPLETE LIST OF PUBLICATIONS

Stavros Tripakis

The PDF file has links to on-line versions of the papers.

EDITED VOLUMES

- [1] Luca Carloni and Stavros Tripakis, editors. *Proceedings of the 10th ACM & IEEE International Conference on Embedded Software, EMSOFT 2010, Scottsdale, AZ, October 25-27, 2010*. ACM, 2010.

REFEREED JOURNAL PAPERS

- [2] Kyungmin Bae, Peter Csaba Olveczky, Thomas Huining Feng, Edward A. Lee, and Stavros Tripakis. Verifying Hierarchical Ptolemy II Discrete-Event Models using Real-Time Maude. *Science of Computer Programming*, Accepted for publication, Oct 2010. <http://www.eecs.berkeley.edu/Pubs/TechRpts/2010/EECS-2010-50.html>.
- [3] S. Tripakis, C. Pinello, A. Benveniste, A. Sangiovanni-Vincentelli, P. Caspi, and M. Di Natale. Implementing Synchronous Models on Loosely Time-Triggered Architectures. *IEEE Transactions on Computers*, 57(10):1300–1314, October 2008. <http://www-verimag.imag.fr/~tripakis/papers/tc08.pdf>.
- [4] S. Tripakis. Checking Timed Büchi Automata Emptiness on Simulation Graphs. *ACM Transactions on Computational Logic*, 10(3):1–19, April 2009. <http://tocl.acm.org/accepted/307tripakis.pdf>.
- [5] M. Krichen and S. Tripakis. Conformance Testing for Real-Time Systems. *Formal Methods in System Design*, 34(3):238–304, June 2009. <http://www-verimag.imag.fr/~tripakis/papers/fmsd09.pdf>.
- [6] F. Cassez and S. Tripakis. Fault Diagnosis with Static or Dynamic Observers. *Fundamenta Informaticae*, 88(4):497–540, 2008. <http://www-verimag.imag.fr/~tripakis/papers/fi08.pdf>.
- [7] S. Bensalem, D. Peled, H. Qu, and S. Tripakis. Automatic Generation of Path Conditions for Concurrent Timed Systems. *Theoretical Computer Science*, 404:275–292, 2008. <http://www-verimag.imag.fr/~tripakis/papers/tcs08.pdf>.
- [8] P. Caspi, N. Scaife, C. Sofronis, and S. Tripakis. Semantics-Preserving Multitask Implementation of Synchronous Programs. *ACM Transactions on Embedded Computing Systems*, 7(2):1–40, February 2008. <http://www-verimag.imag.fr/~tripakis/papers/acm-tecs08.pdf>.
- [9] S. Tripakis. Folk Theorems on the Determinization and Minimization of Timed Automata. *Information Processing Letters*, 99(6):222–226, September 2006. <http://www-verimag.imag.fr/~tripakis/papers/ipl06.pdf>.

- [10] S. Tripakis, C. Sofronis, P. Caspi, and A. Curic. Translating Discrete-Time Simulink to Lustre. *ACM Transactions on Embedded Computing Systems*, 4(4):779–818, November 2005. <http://www-verimag.imag.fr/~tripakis/papers/acm-tecs05.pdf>.
- [11] S. Tripakis, S. Yovine, and A. Bouajjani. Checking Timed Büchi Automata Emptiness Efficiently. *Formal Methods in System Design*, 26(3):267–292, May 2005. <http://www-verimag.imag.fr/~tripakis/papers/fmsd05.pdf>.
- [12] S. Tripakis. Decentralized Control of Discrete Event Systems with Bounded or Unbounded Delay Communication. *IEEE Transactions on Automatic Control*, 49(9):1489–1501, September 2004. <http://www-verimag.imag.fr/~tripakis/papers/tac04.pdf>.
- [13] S. Tripakis. Undecidable Problems of Decentralized Observation and Control on Regular Languages. *Information Processing Letters*, 90(1):21–28, April 2004. <http://www-verimag.imag.fr/~tripakis/papers/ipl04.pdf>.
- [14] J. Sifakis, S. Tripakis, and S. Yovine. Building Models of Real-Time Systems from Application Software. *Proceedings of the IEEE, Special issue on Modeling and Design of Embedded Software*, 91(1):100–111, January 2003. <http://www-verimag.imag.fr/~tripakis/papers/ieee03.pdf>.
- [15] S. Tripakis and S. Yovine. Analysis of Timed Systems using Time-abstracting Bisimulations. *Formal Methods in System Design*, 18(1):25–68, January 2001. <http://www-verimag.imag.fr/~tripakis/papers/fmsd01.pdf>.

REFEREED CONFERENCE PAPERS

- [16] Edward A. Lee and Stavros Tripakis. Modal Models in Ptolemy. In *EOOLT 2010 – 3rd International Workshop on Equation-Based Object-Oriented Modeling Languages and Tools*. Linköping University Electronic Press, October 2010. **Voted Best Paper**. <http://chess.eecs.berkeley.edu/pubs/700.html>.
- [17] S. Tripakis, C. Stergiou, and R. Lublinerman. Checking Non-Interference in SPMD Programs. In *2nd USENIX Workshop on Hot Topics in Parallelism (HotPar'10)*, pages 1–5, June 2010. <http://chess.eecs.berkeley.edu/pubs/663.html>.
- [18] S. Tripakis, B. Lickly, T.A. Henzinger, and E.A. Lee. On Relational Interfaces. In *Proceedings of the 9th ACM & IEEE International Conference on Embedded Software (EMSOFT'09)*, pages 67–76. ACM, 2009. <http://www-verimag.imag.fr/~tripakis/papers/emsoft09.pdf>.
- [19] K. Bae, P.C. Olveczky, T.H. Feng, and S. Tripakis. Verifying Ptolemy II Discrete-Event Models using Real-Time Maude. In *Formal Methods and Software Engineering: 11th International Conference on Formal Engineering Methods (ICFEM'09)*, 2009. <http://www-verimag.imag.fr/~tripakis/papers/icfem09.pdf>.
- [20] M-K. Leung, T. Mandl, E.A. Lee, E. Latronico, C. Shelton, S. Tripakis, and B. Lickly. Scalable Semantic Annotation using Lattice-based Ontologies. In *12th Intl. Conf. Model Driven Engineering Languages and Systems (MODELS 2009)*, 2009. **ACM SIGSOFT Distinguished Paper Award**. <http://chess.eecs.berkeley.edu/pubs/611.html>.

- [21] S. Tripakis. A Combined On-line/Off-line Framework for Black-Box Fault Diagnosis. In *Runtime Verification*, volume 5799 of *LNCS*, pages 152–167. Springer, September 2009. <http://www-verimag.imag.fr/~tripakis/papers/rv09.pdf>.
- [22] A. Benveniste, P. Caspi, R. Lubliner, and S. Tripakis. Actors without Directors: a Kahnian View of Heterogeneous Systems. In *HSCC'09: Proceedings of the 12th International Conference on Hybrid Systems: Computation and Control*, LNCS, pages 46–60. Springer, 2009. <http://www-verimag.imag.fr/~tripakis/papers/hsc09.pdf>.
- [23] R. Lubliner, C. Szegedy, and S. Tripakis. Modular Code Generation from Synchronous Block Diagrams – Modularity vs. Code Size. In *36th ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages (POPL'09)*, pages 78–89. ACM, January 2009. <http://www-verimag.imag.fr/~tripakis/papers/pop109.pdf>.
- [24] R. Lubliner and S. Tripakis. Translating Data Flow to Synchronous Block Diagrams. In *IEEE/ACM/IFIP Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia'08)*. IEEE, 2008. <http://www-verimag.imag.fr/~tripakis/papers/estimedia08.pdf>.
- [25] N. Abed, S. Tripakis, and J-M. Vincent. Resource-Aware Verification Using Randomized Exploration of Large State Spaces. In *SPIN'08*, number 5156 in LNCS, pages 214–231, 2008. <http://www-verimag.imag.fr/~tripakis/papers/spin08.pdf>.
- [26] F. Cassez and S. Tripakis. Fault diagnosis with dynamic observers. In *9th Intl. Workshop on Discrete Event Systems (WODES'08)*, pages 212–217. IEEE, May 2008. <http://www-verimag.imag.fr/~tripakis/papers/wodes08.pdf>.
- [27] R. Lubliner and S. Tripakis. Modular Code Generation from Triggered and Timed Block Diagrams. In *14th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'08)*, pages 147–158. IEEE CS Press, April 2008. <http://www-verimag.imag.fr/~tripakis/papers/rtas08.pdf>.
- [28] R. Lubliner and S. Tripakis. Modularity vs. Reusability: Code Generation from Synchronous Block Diagrams. In *Design, Automation, and Test in Europe (DATE'08)*, pages 1504–1509. ACM, March 2008. <http://www-verimag.imag.fr/~tripakis/papers/date08.pdf>.
- [29] M. Di Natale, A. Benveniste, P. Caspi, C. Pinello, A. Sangiovanni-Vincentelli, and S. Tripakis. Applying LTTA to guarantee flow of data requirements in distributed systems using Controller Area Networks. DATE Workshop on Dependable Software Systems, 2008. http://www-verimag.imag.fr/~tripakis/papers/DATE_WS08.pdf.
- [30] S. Bensalem, D. Peled, H. Qu, S. Tripakis, and L. Zuck. Test Case Generation for Ultimately Periodic Paths. In *Haifa Verification Conference (HVC'07)*, volume 4899 of LNCS. Springer, October 2007. <http://www-verimag.imag.fr/~tripakis/papers/hvc07.ps>.
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