Challenges in multi-core implementation of critical data-flow applications

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Verimag
- Methods and Tools for Safe and Secure Cyber-Physical Systems
- Organized in themes:
  - Shared Resources

Kalray
- Fabless design of many-core VLIW processors
- Created in 2008, spin-off from CEA and ST
- 3rd generation of the MPPA with 80 cores and 5 clusters
Critical applications

- Control systems are omnipresent in our age
  - Planes, Cars, Trains, Nuclear Plants, ...

- **Hard Real Time-Systems**
  - The tasks should finish within reliable time bounds
  - System fails if deadline is missed
Application Model

**Synchronous Data-Flow Languages**

- Abstracted as a Directed Acyclic Graph (DAG)
- Precedence and communication
- Examples: Lustre, SCADE, Blech

![Diagram of a Directed Acyclic Graph (DAG)](image-url)
From Data-Flow to Multi/Many-Core

Challenges

- Parallelism extraction
- Communication
- Synchronization

Mapping and Scheduling:
- #cores
- order

Complete system orchestration
Interference in a nutshell

Challenges

- Correctly evaluate the interference delay
- Compute the overall timing impact
Execution Models

Single-Phase

\[ N_1 \quad (R+Ex+W) \]

2-Phased

\[ N_1 \quad (R+Ex) \quad WN_1 \]

3-Phased

\[ RN_1 \quad ExN_1 \quad WN_1 \]

Challenges

- Is it worth to split the tasks?
- Find a good model that matches the target architecture
  - Memory hierarchy
  - Memory access arbitration
Conclusion

- Non-trivial problem
  - Multi/Many-core platforms
  - Critical applications
- There is no off-the-shelf answer
  - Everything is a compromise between *complexity* and *precision*
  - Incorporating the hardware knowledge eases the approach

Ongoing challenges

- Interference Analysis
- Execution Models
- Integration with industrial tools

Future challenges

- Mapping and Scheduling
- Many-Core scalability
- Generic methodology
Publications


Thanks for your attention!

Questions?

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MPPA3 Coolidge overview

**COOLIDGE PROCESSOR**
5 compute clusters at 1200 MHz
2x 100Gbps Ethernet, 16x PCIe Gen4

**COMPUTE CLUSTER**
16+1 cores, 4 MB local memory
NoC and AXI global interconnects

**6-ISSUE VLIW CORE**
64x 64-bit register file
128MAC/c tensor coprocessor
Timing Analysis

- Knowledge of hardware: MPPA2 / MPPA3
- Knowledge of software: Synchronous Data-Flow
- Time-triggered execution: interference control
- Development and use of the Multi-Core Interference Analysis (MIA) tool\(^1\)

\(^1\)Open source software available under the CeCILL-C license
https://gricad-gitlab.univ-grenoble-alpes.fr/verimag/synchrone/mia
# Multi-Core Interference Analysis

## Inputs
- Initial release date of tasks
- Period and deadline
- Dependencies between the tasks
- WCET in isolation + WC number of accesses

## Outputs
- Schedulable / Not Schedulable
- Final release dates of tasks
  - Minimize interference
  - Predictable runtime