Hamza Rihani

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Research Interests

Timing analysis, including scheduling and execution time, of parallel applications running on many-core processors, particularly in the field of real-time systems.

Professional Experience

December 14 – Present

Grenoble, France

Verimag Lab, Full Time Researcher

I work within a collaborative project with industrial and academic partners. My contributions target Kalray's many-core processors (`http://www.kalrayinc.com/`)

February 2014 – July 2014

Walldorf, Germany

SAP AG, Master's Thesis

Title: Adaptive Lock Elision in Hardware Transactional Memory.
The goal of this project was to understand the intricate details of Intel TSX instructions for Hardware Transactional Memory, and investigate how to apply them to basic data structures of SAP HANA in order to simplify them and/or improve their performance under high concurrency.
Used language: C++

March 2013 – August 2013

Walldorf, Germany

SAP AG, Master's Internship

Title: Compression using hardware acceleration.
I investigated and evaluated a new compression card delivered as proof-of-concept. The goal of my project was to accelerate the compression inside the SAP HANA In-Memory Database using this hardware. In order to improve the performance, I also parallelized the compression phase. Through my work, I achieved a significant speedup.
Used language: C++.

June 2012 – August 2012

Tokyo, Japan

National Institute of Informatics, Research Intern

Title: Human Imitation Behavior.
I developed a module of imitation process using stereo vision into a simulator software. SIGVerse [sigverse.org] is a project developed by Inamura Laboratory. It provides different environments that aims for research on genesis of social intelligence.
Used language: C++.

Education

Dec. 2014 – present

Ph.D candidate

Verimag lab/Univ. Grenoble Alpes

Topic: Timing analysis on many-core processors and its applications to the Kalray MPPA-256 platform.
Expected graduation: November, 2017
Advisors: Matthieu Moy, Claire Maiza.

2013 – 2014

Master of Science in Informatics (by research)

Joseph Fourier University, France

Degree: Master of Science by Research.
Major: Parallel, Distributed and Embedded Systems.

2011 – 2013

Titre d'Ingénieur (Master in Computer Science)

Grenoble INP - Ensimag, France

Degree: Titre d'Ingénieur (eq. Master of Science) in Computer Science.
Major: Embedded Systems and Software.

2010 – 2011

Bachelor's degree in Engineering Sciences

Université Henri Poincaré, France

Degree: Bachelor's degree.

2007 – 2010

Undergraduate Studies in Engineering Sciences

ENPEI - Rouiba, Algeria

Degree: Undergraduate Scientific Degree.

Software Skills

Programming	C++, C, Java, Python, Bash, x86 Assembly, Low level programming, Parallel programming
Operating Systems	Linux, Windows
Software	Eclipse, Git, Vim, LaTeX, R, Word, Excel
Profiling	Intel® VTune, GDB, Valgrind, Linux Perf
Simulation	Matlab, Simulink

Communication Skills

English	Fluent (TOEIC: 930pts)
French	Fluent
Arabic	Native language
Spanish	Beginner
Japanese	Beginner

Publications

- H. Rihani, M. Moy, C. Maiza, R. I. Davis, S. Altmeyer, "Response Time Analysis of Synchronous Data Flow Programs on a Many-core Processor". In proceedings of the *24th International Conference on Real-Time Networks and Systems (RTNS), 2016*
- H. Rihani, C. Maiza, M. Moy, "Efficient Execution of Dependent Tasks on Many-Core Processors". In the *Real-Time Scheduling Open Problems Seminar (RTSOPS), 2016*
- H. Rihani, M. Moy, C. Maiza and S. Altameyer: WCET Analysis in Shared Resources Real-Time Systems with TDMA Buses. In proceedings of the *23rd International Conference on Real-Time Networks and Systems (RTNS), 2015*
- H. Rihani, P. Sanders and R. Dementiev: Brief Announcement: MultiQueues: Simple Relaxed Concurrent Priority Queues. In the *27th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA), 2015*

Training

August 2015

Ecole Temps-Réel (Real-Time School), 6 days, Rennes, France

July 2015

11th Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems, 5 days, Fiuggi, Italy

June 2015

3rd Summer School on Critical Embedded Systems, 5 days, Toulouse France

Academic Community Activities

Journal Reviewing

- Journal of Systems Architecture (JSA)

Conference Reviewing

- International Conference on Design, Automation and Test in Europe (DATE) 2017
- International Conference on Real-Time Networks and Systems (RTNS) 2016
- International Workshop on Worst-Case Execution Time Analysis (WCET) 2016

Program Committee

- Junior Researcher Workshop on Real-Time Computing (JRWRTC) 2016

Extracurricular Activities

- Former member of the Bug Buster service at Ensimag (from September 2012 to January 2013). My mission was to provide an IT support service for students personal laptops.
- Former member of the Mechanic Club and the Equestrian Club at ENPEI.
- Reading: Whodunit, Fantasy
  Favorite authors: Sir Arthur Conan Doyle,
  Agatha Christie, Maurice Leblanc, George R.R Martin
- Sports: Jogging, Biking, Hiking
- Traveling: Visited several countries across Europe, Japan, and Tunisia

References

Available upon request