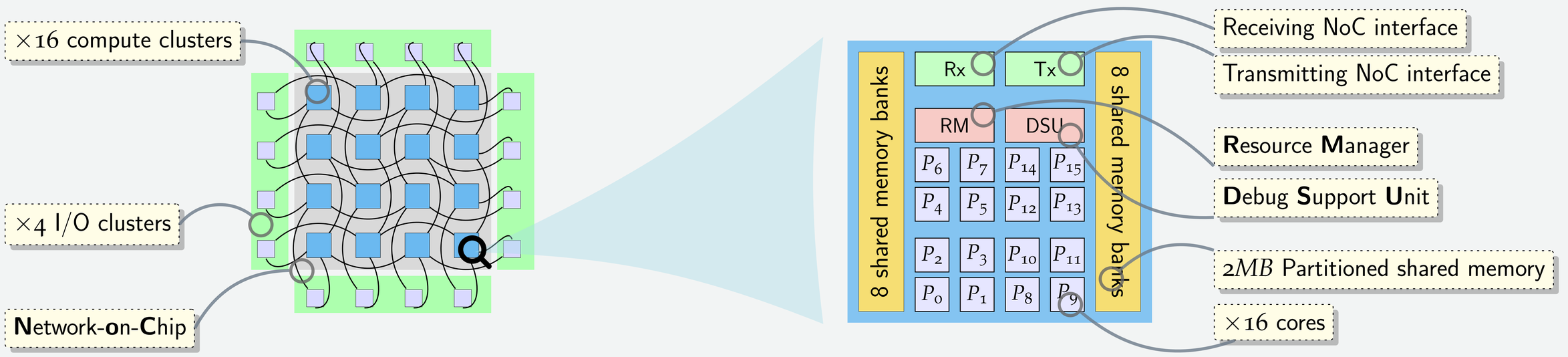
Interference Analysis on Kalray MPPA-256

Kalray MPPA-256: A Many-core Processor*

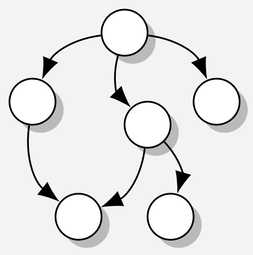


Massively parallel processor with low power consumption and a predictable design

* 2nd generation code-named *Bostan*

1. Dependent Task Graph Model

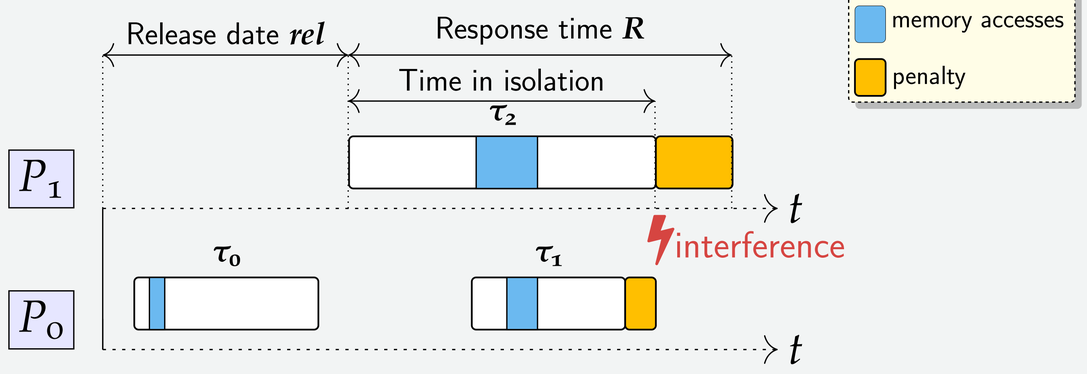
- Represented as a **D**irect **A**cyclic **G**raph
- Execution order constrained by task dependencies



↪ **Applications:** automotive, avionics,...

In static scheduling, tasks are released only after all their dependencies finish

2. Interference Effects

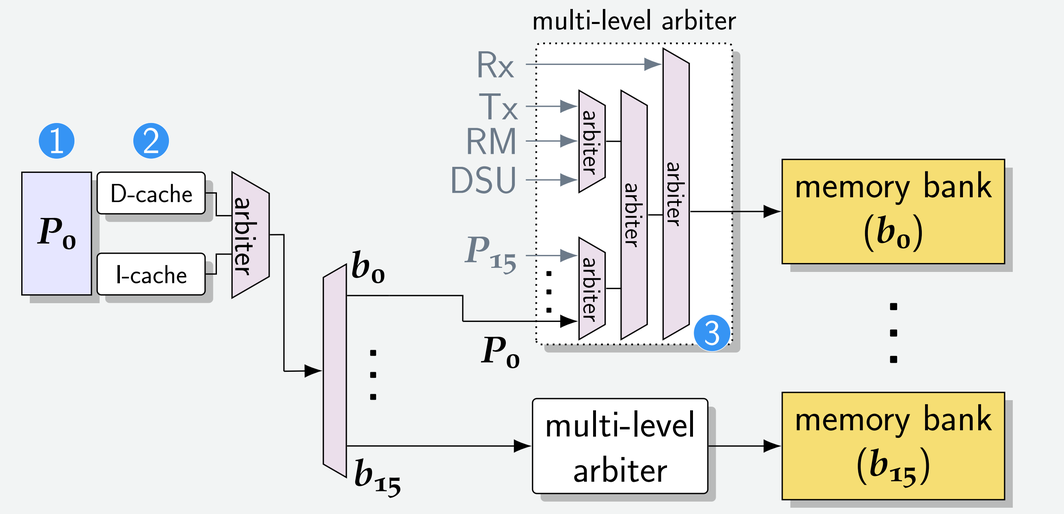


↪ **Observations**

- Task τ_0 runs alone on the processor without a penalty
- Tasks τ_1 and τ_2 run concurrently and interfere

Interference depends on *release dates* and *response times*

3. Sources of Interference



1. Preemption from higher priority tasks
2. **C**ache **R**elated **P**reemption **D**elay due to changes of cache contents
3. Bus interference depending on the arbitration policy

↪ **Response Time Equation**

Considering a task set $\Gamma = \{\tau_0, \ldots, \tau_n\}$

Response time of task τ_i — Response times of Γ $\mathcal{R} = \{R_0, \ldots, R_n\}$ — Release dates of Γ $\Theta = \{rel_0, \ldots, rel_n\}$

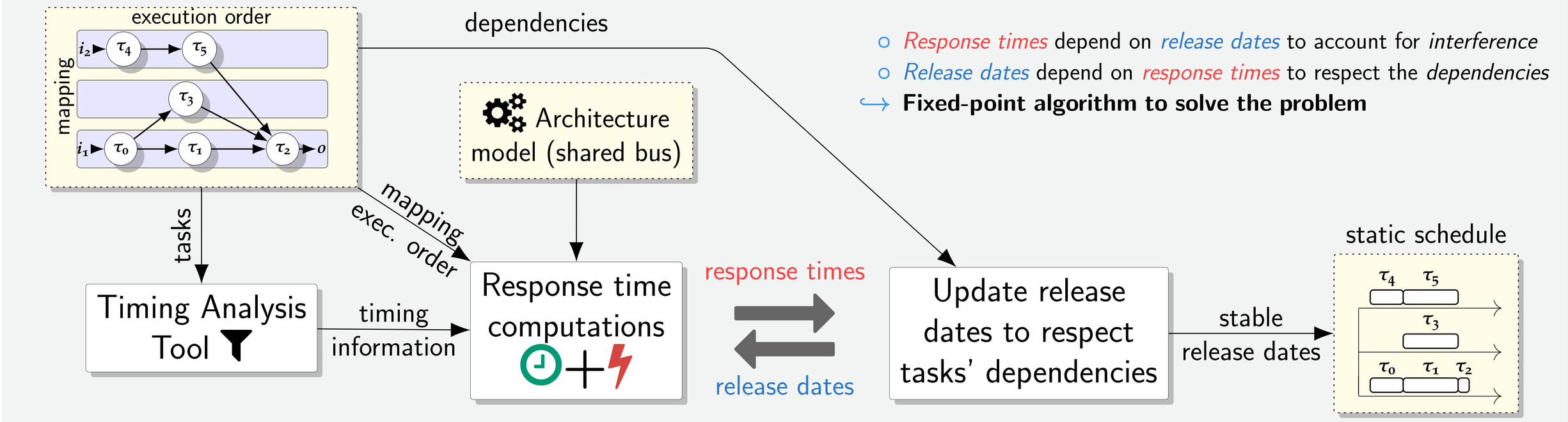
$$\forall i : R_i = \mathbf{WCET}_i + \underbrace{I^{\mathbf{CORE}}(\mathcal{R}, \Theta) + I^{\mathbf{CRPD}}(\mathcal{R}, \Theta)}_{\text{Interference due to preemption}} + \underbrace{\sum_{b \in \{b_0, \ldots, b_{15}\}} I_b^{\mathbf{BUS}}(\mathcal{R}, \Theta)}_{\text{Bus interference on memory bank } b}$$

Time in isolation

↪ **Assumptions**

- Non-preemptive static scheduling: $I^{\mathbf{CORE}} = I^{\mathbf{CRPD}} = 0$

4. Response Time Analysis Framework



- *Response times* depend on *release dates* to account for *interference*
- *Release dates* depend on *response times* to respect the *dependencies*

↪ **Fixed-point algorithm to solve the problem**

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References

[1] B. D. de Dinechin, D. van Amstel, M. Poulhiès, and G. Lager. "Time-critical computing on a single-chip massively parallel processor". In *DATE'14*

[2] H. Rihani, M. Moy, C. Maiza, R. I. Davis, S. Altmeyer, "Response Time Analysis of Synchronous Data Flow Programs on a Many-core Processor". In *RTNS'16*