Habilitation à Diriger des Recherches High-level Models for Embedded Systems

Matthieu Moy

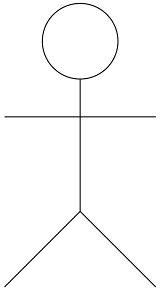
Verimag (Grenoble INP)
Grenoble, France

March 13th 2014

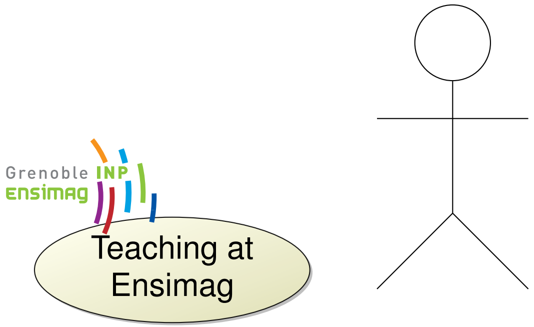
Jury:

Gérard Berry	Professeur au Collège de France	Reviewer
Rolf Drechsler	Professor at TU Bremen, Germany	Reviewer
Marco Roveri	Senior Researcher, Fondazione Bruno Kessler, Italy	Reviewer
Samarjit Chakraborty	Professor at TU Muchen, Germany	Examiner
Benoît Dupont de Dinechin	Directeur Technique, Kalray, France	Examiner
Frédéric Pétrot	Professeur à Grenoble INP, France	Examiner

About Me



About Me



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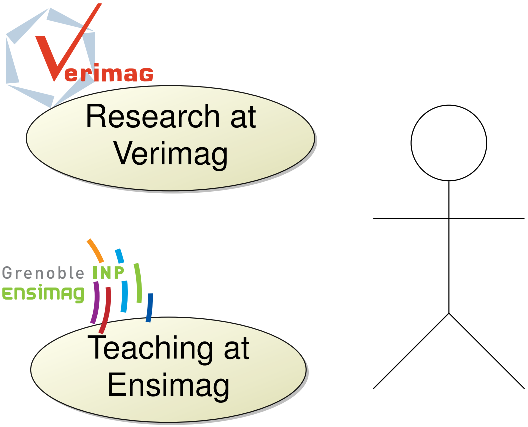

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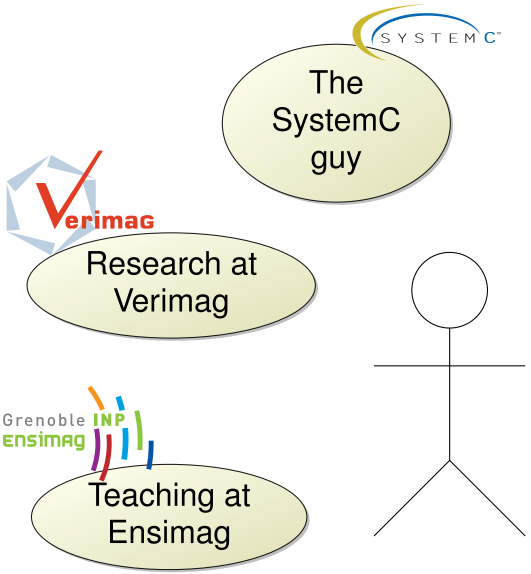
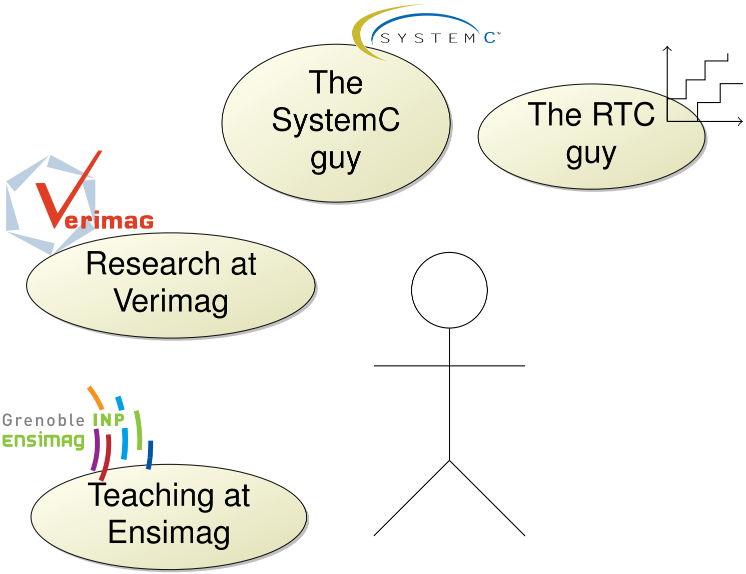

SYSTEMC
The SystemC guy
Verimag
Research at Verimag
Grenoble INP Ensimag
Teaching at Ensimag

About Me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The RTC guy
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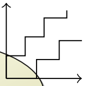
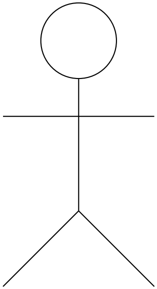
The RTC guy



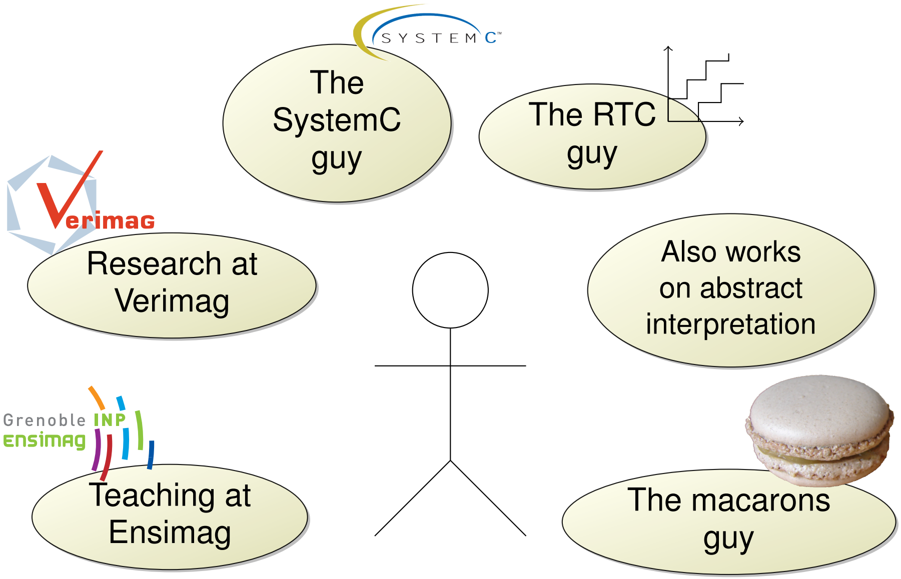
Research at Verimag

Also works on abstract interpretation



Teaching at Ensimag

About Me


SYSTEMC
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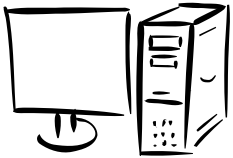
Grenoble INP Ensimag
Teaching at Ensimag
The macarons guy

What Are Processors For?

Computers



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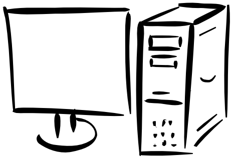
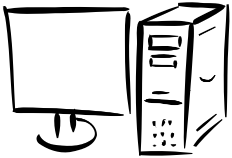
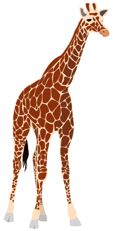


Embedded systems

What Are Processors For?

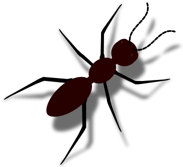
Computers





Vertebrate

Embedded systems

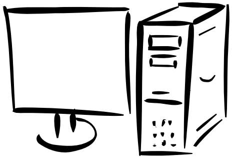


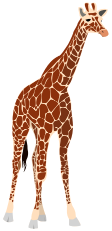
Insects

Source: `http://skepchick.org/2013/03/planet-of-the-arthropods/`

What Are Processors For?

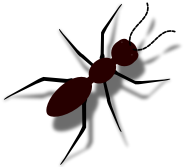
Computers
≈ 2%





Vertebrate
≈ 4%

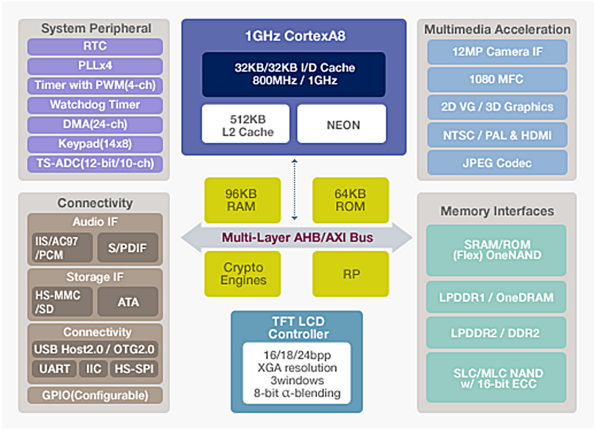
Embedded
systems
≈ 98%



Insects
≈ 96%

Source: `http://skepchick.org/2013/03/planet-of-the-arthropods/`

Prehistory: My Phone (2010)



Source: `http://www.embeddedinsights.com/epd/samsung/samsung-s5pc110.php`

Another Typical Embedded System: my New Camera

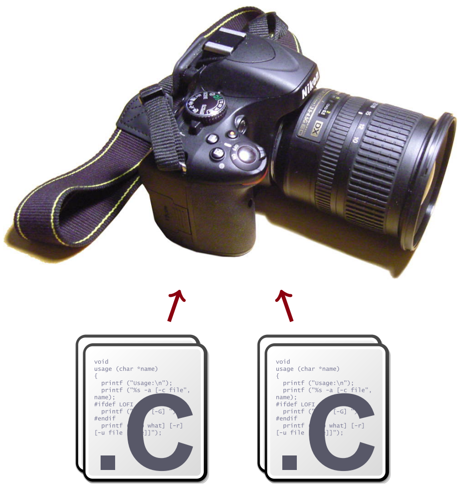
Another Typical Embedded System: my New Camera

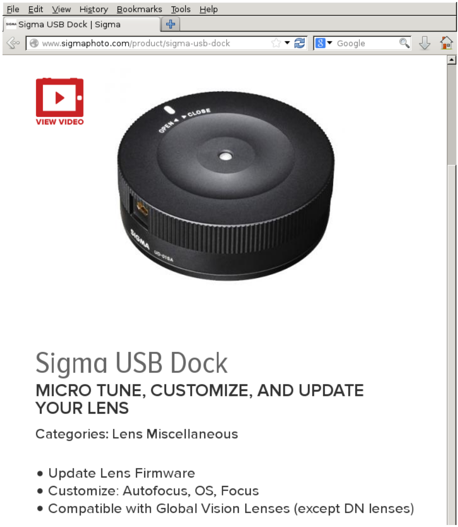
Firmware

Another Typical Embedded System: my New Camera

Firmware A
Firmware B

Another Typical Embedded System: my New Camera




File Edit View History Bookmarks Tools Help
Sigma USB Dock | Sigma
www.sigmaphoto.com/product/sigma-usb-dock
Google
VIEW VIDEO

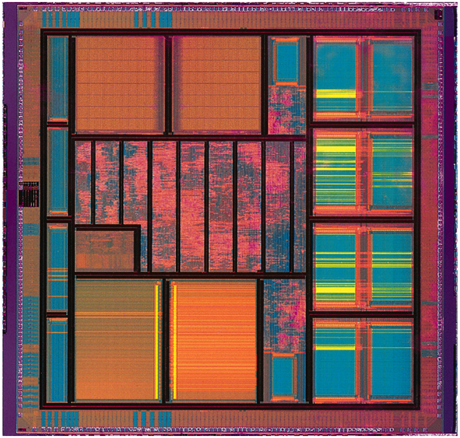
Sigma USB Dock

MICRO TUNE, CUSTOMIZE, AND UPDATE YOUR LENS

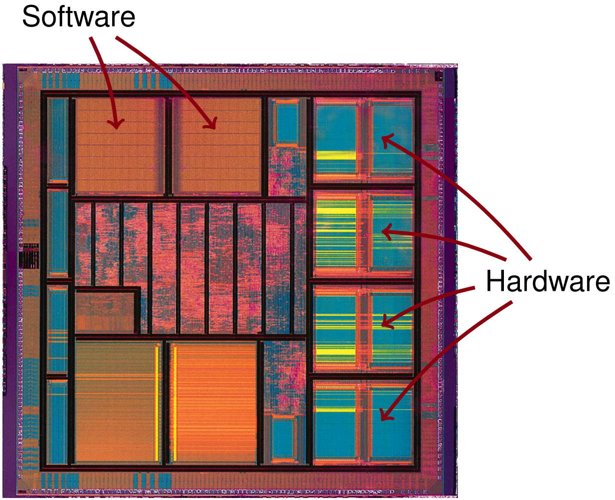
Categories: Lens Miscellaneous

- Update Lens Firmware
- Customize: Autofocus, OS, Focus
- Compatible with Global Vision Lenses (except DN lenses)

Modern Systems-on-a-Chip



Modern Systems-on-a-Chip



Issue 1: Functional Correctness

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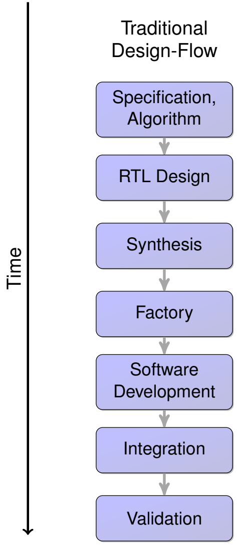
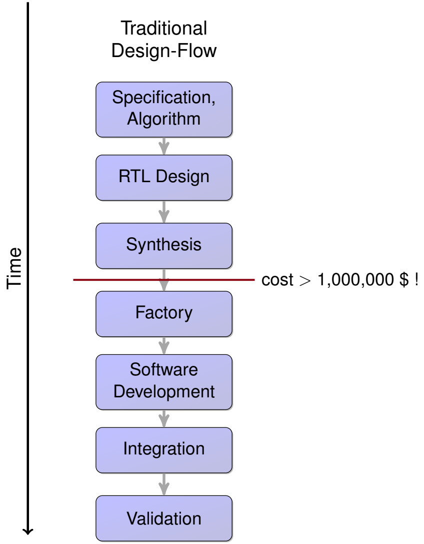
$\downarrow$

Issue 1: Functional Correctness

Issue 2: Early Software Development



Issue 2: Early Software Development



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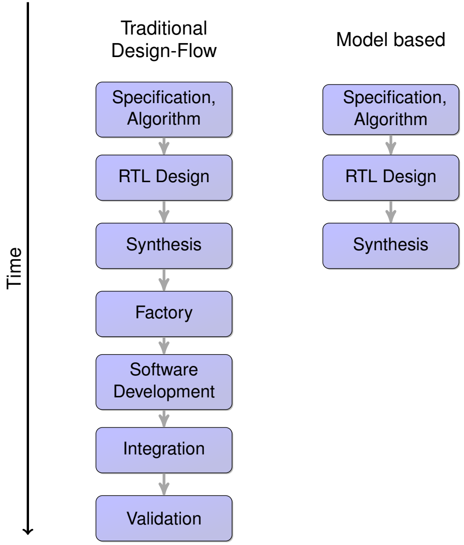

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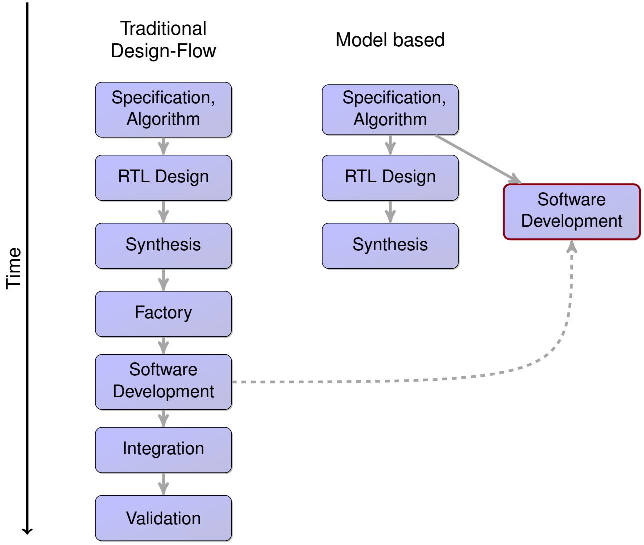

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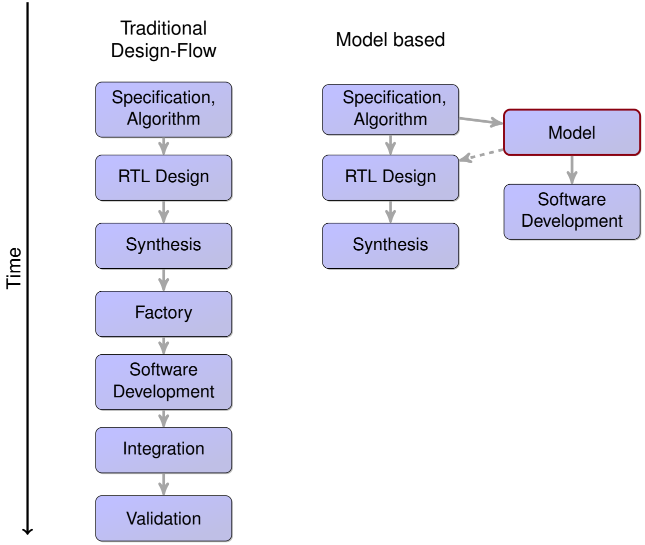

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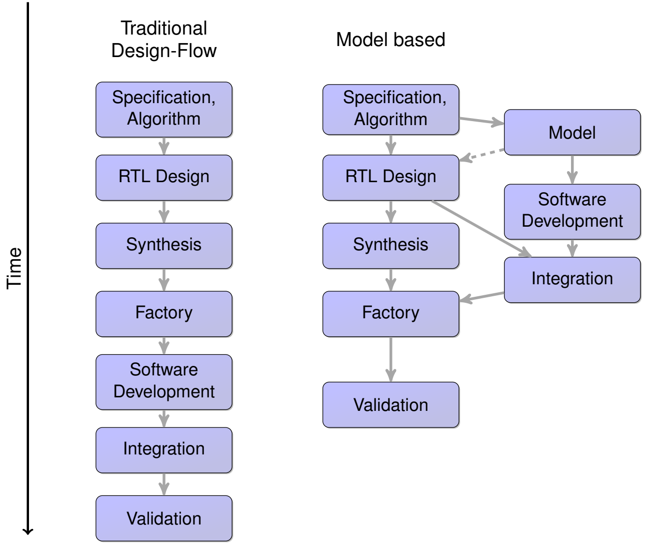

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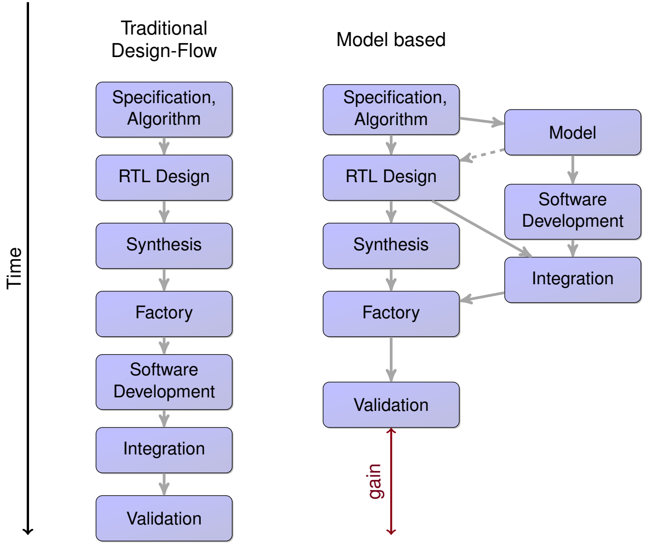
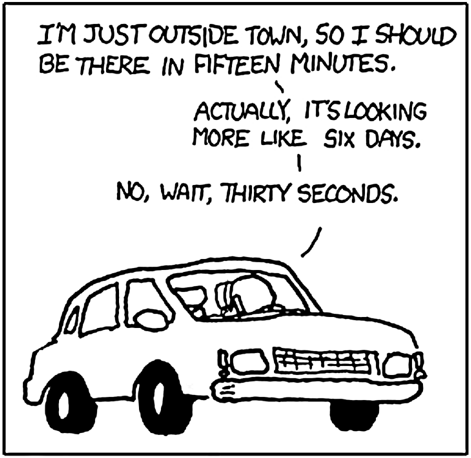
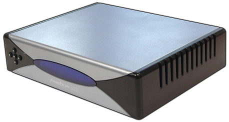


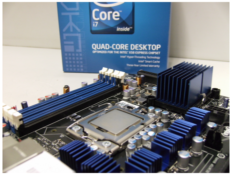
Issue 3: Timing


I'M JUST OUTSIDE TOWN, SO I SHOULD BE THERE IN FIFTEEN MINUTES.
ACTUALLY, IT'S LOOKING MORE LIKE SIX DAYS.
NO, WAIT, THIRTY SECONDS.

THE AUTHOR OF THE WINDOWS FILE COPY DIALOG VISITS SOME FRIENDS.

Issue 4: Power and Temperature





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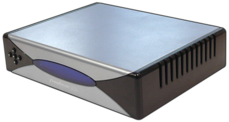
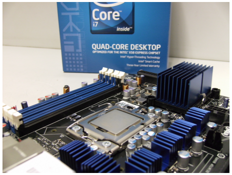
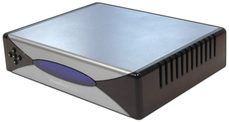
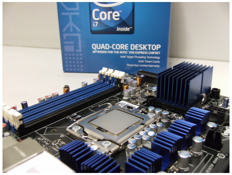




50-130 watt

Issue 4: Power and Temperature

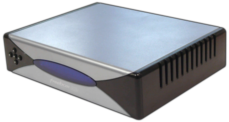




50-130 watt

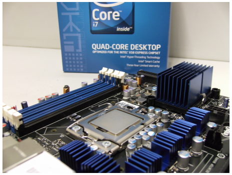
20-30 watt

Issue 4: Power and Temperature



20 watt

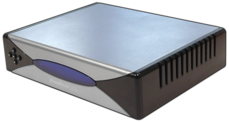
20-30 watt



50-130 watt

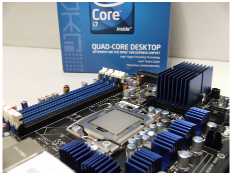
Issue 4: Power and Temperature

$<$ 1 watt



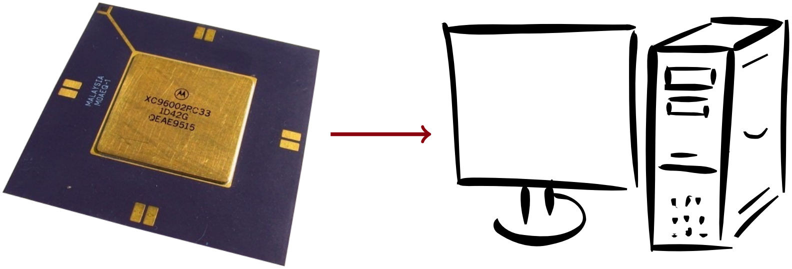
20 watt

20-30 watt

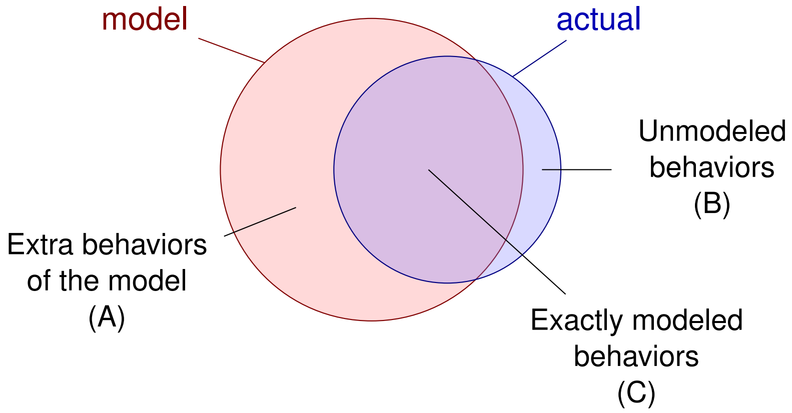


50-130 watt

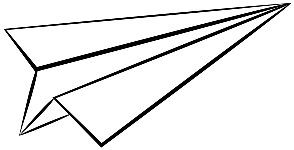
Issue 5: Simulation speed



Issue 6: Model Faithfulness


model
actual
Unmodeled behaviors (B)
Extra behaviors of the model (A)
Exactly modeled behaviors (C)

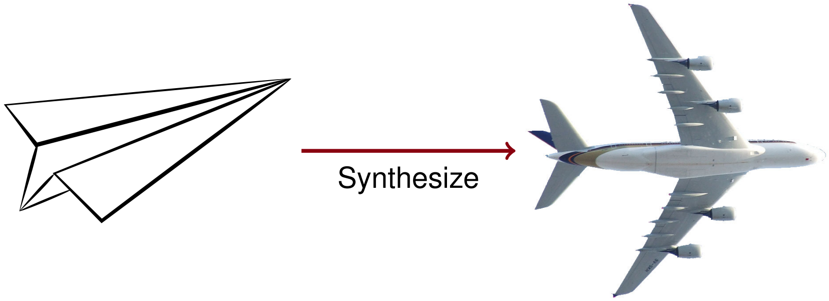
Models and Virtual Prototypes



Model/Prototype

Real system

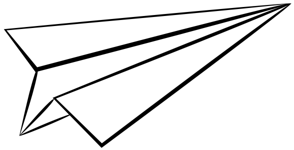
Models and Virtual Prototypes



Model/Prototype

Real system

Models and Virtual Prototypes



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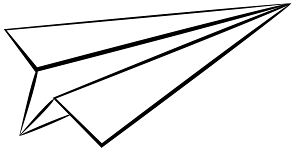
(Synthesize)

Model/Prototype

Real system

Models and Virtual Prototypes

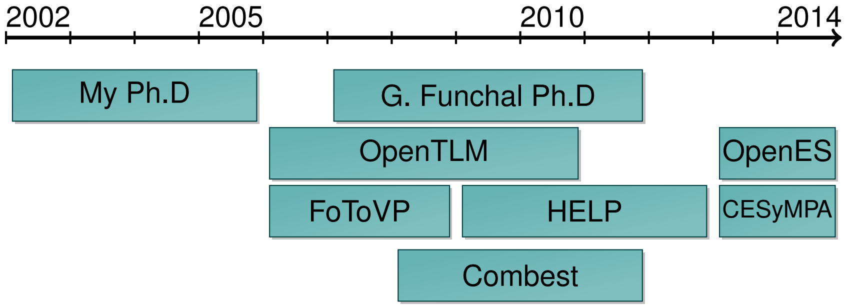


(Synthesize)
Compare
Use as specification
...

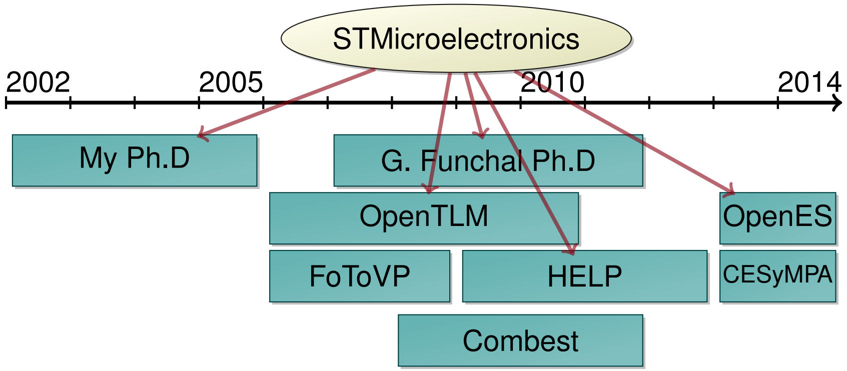
Model/Prototype

Real system

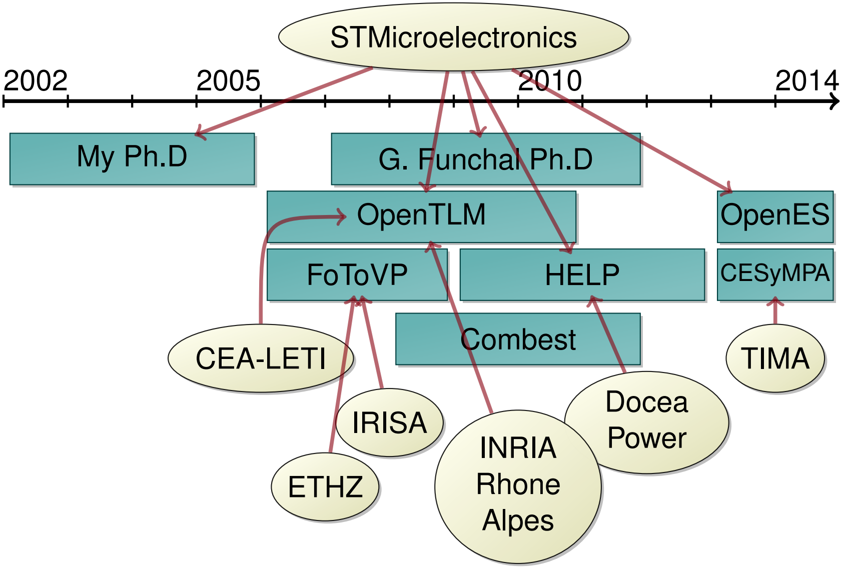
Context and Collaborations of my Work



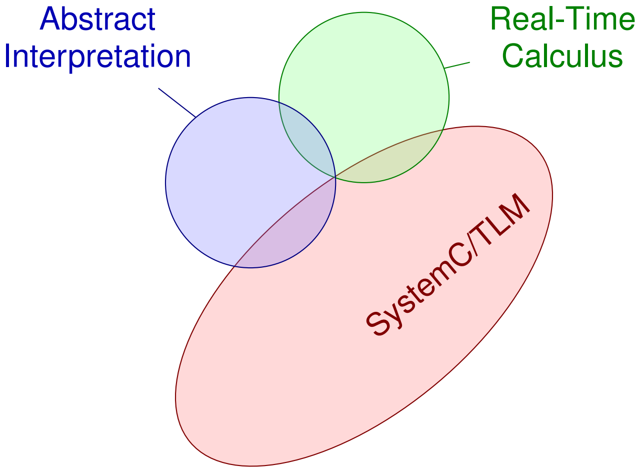
Context and Collaborations of my Work



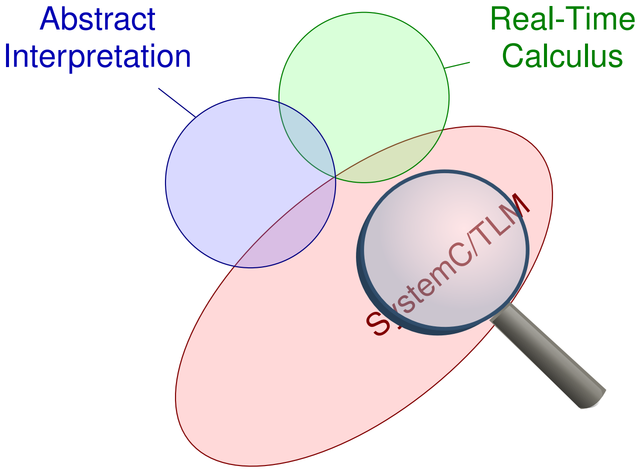
Context and Collaborations of my Work



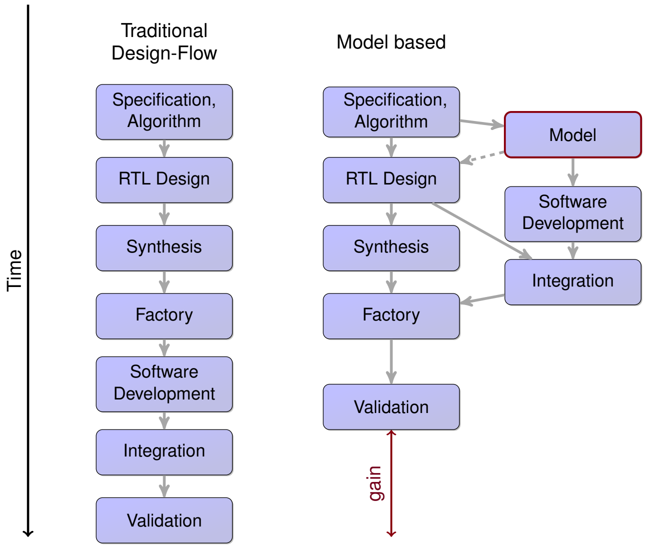
Outline



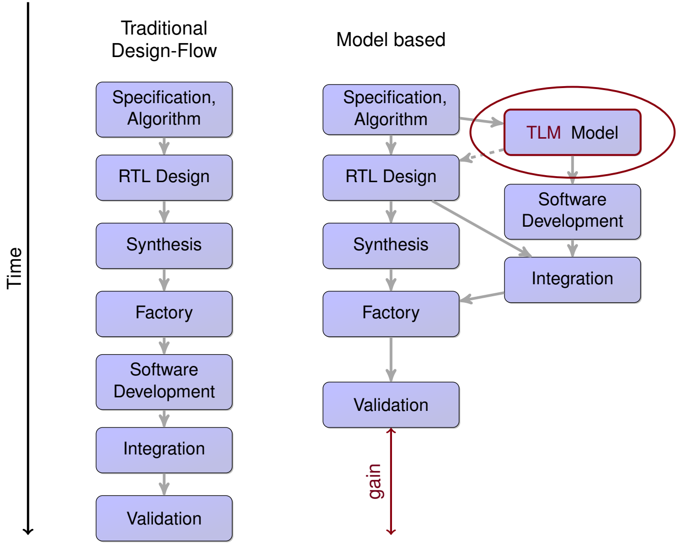
Outline



TLM and Software Development



TLM and Software Development



The Transaction Level Model (TLM): Principles and Objectives

A high level of abstraction,
that appears early in the design-flow

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$\approx$ 1000 Faster than
low-level simulations (RTL)

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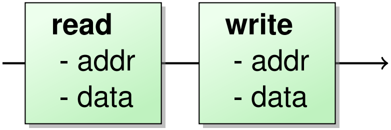
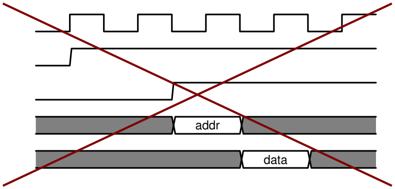
In production in the industry

Content of a TLM Model

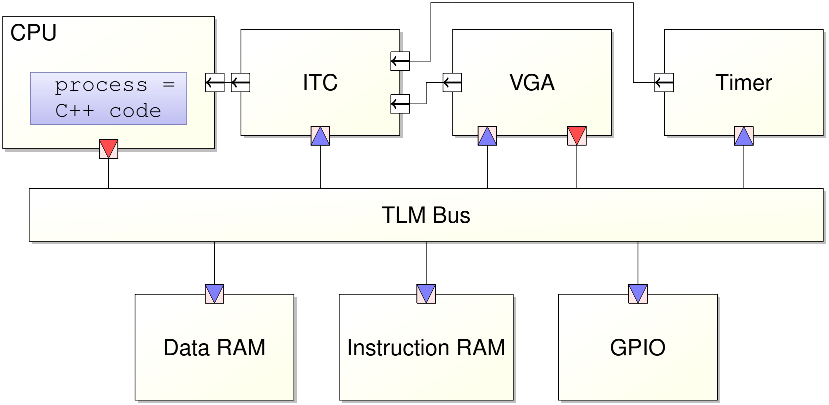
- Model what is needed for Software Execution:
  - Processors
  - Address-map
  - Concurrency
- ... and only that.
  - No micro-architecture
  - No bus protocol
  - No pipeline
  - No physical clock
  - . . .





Standard for TLM = SystemC (IEEE1666)

An Example TLM Model



Uses of Functional Models

Reference for Hardware Validation

Virtual Prototype for Software Development

Uses of Functional Models

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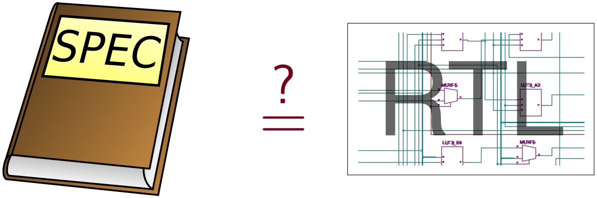

Virtual Prototype for Software Development

Uses of Functional Models

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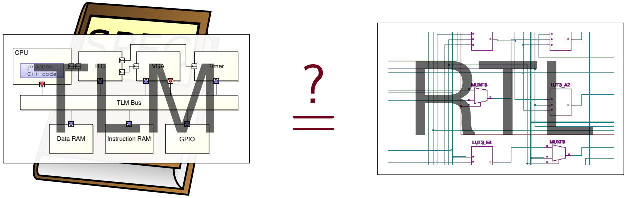

Virtual Prototype for Software Development

Uses of Functional Models

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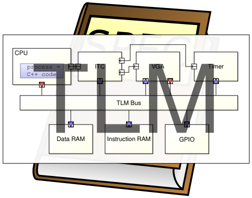

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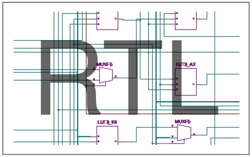

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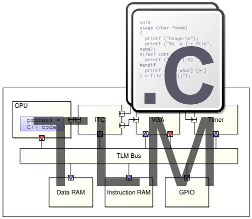
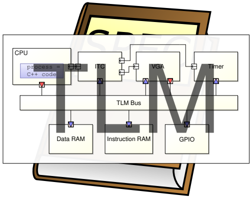


```
void
usage (char *name)
{
  printf ("Usage:\n");
  printf ("%s -a [-c file",
name);
#ifdef LOFI
  printf ("[illegible] [-G] ");
#endif
  printf ([illegible] what] [-r]
[-u file [illegible]]");
```

Uses of Functional Models

Reference for Hardware Validation



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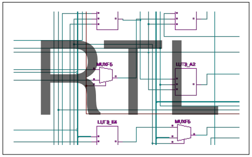
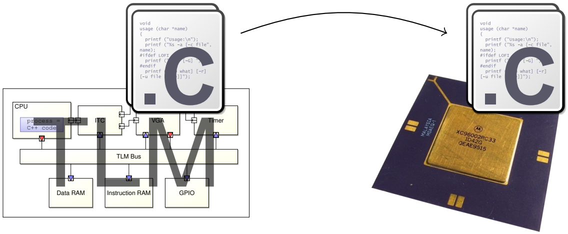


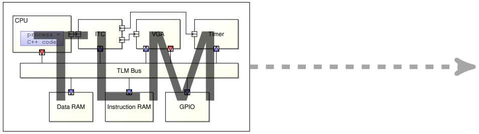
Unmodified Software

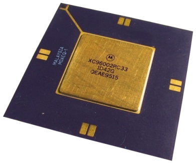
Virtual Prototype for Software Development



Non-Functional Models

Timing, Power consumption, Temperature Estimation





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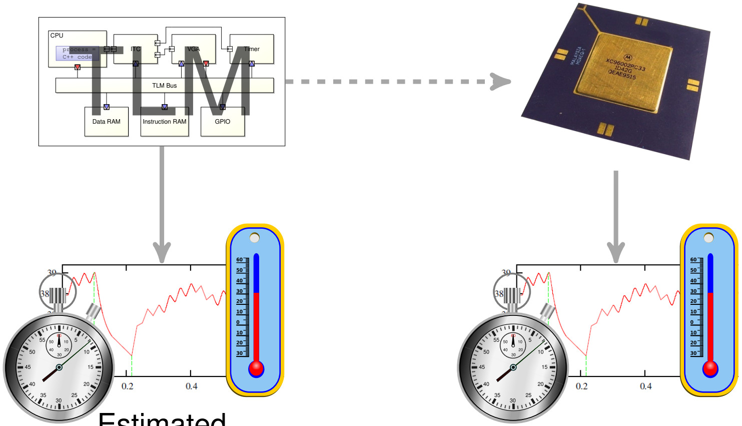
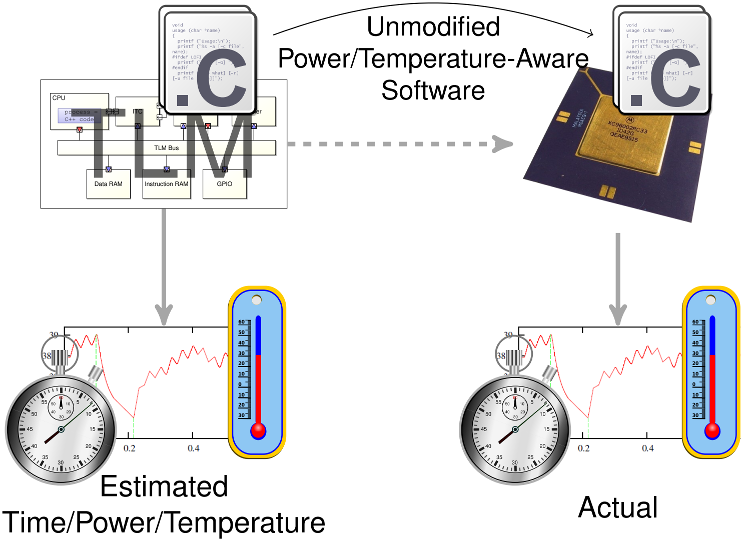


Estimated
Time/Power/Temperature

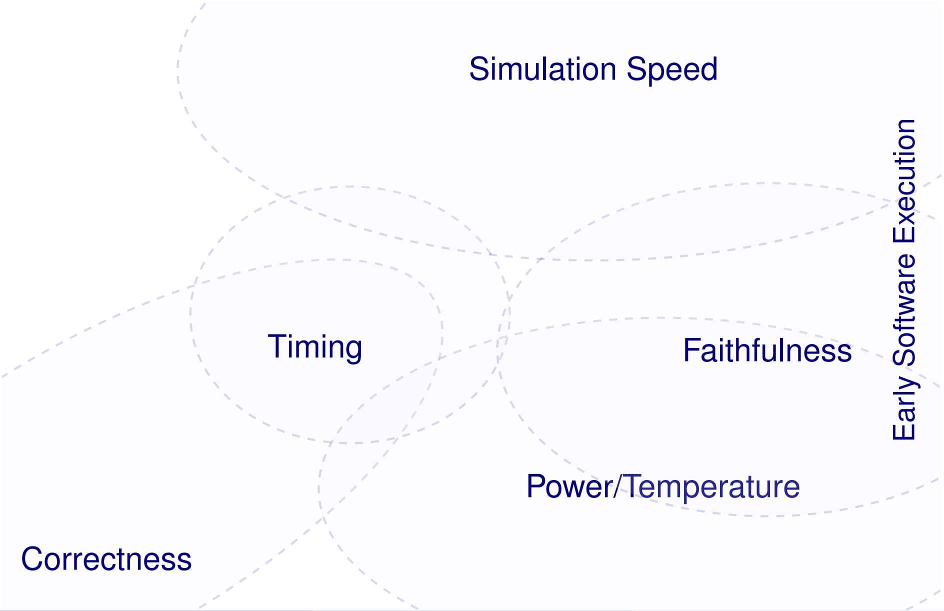
Actual

Non-Functional Models

Timing, Power consumption, Temperature Estimation



Contributions on TLM



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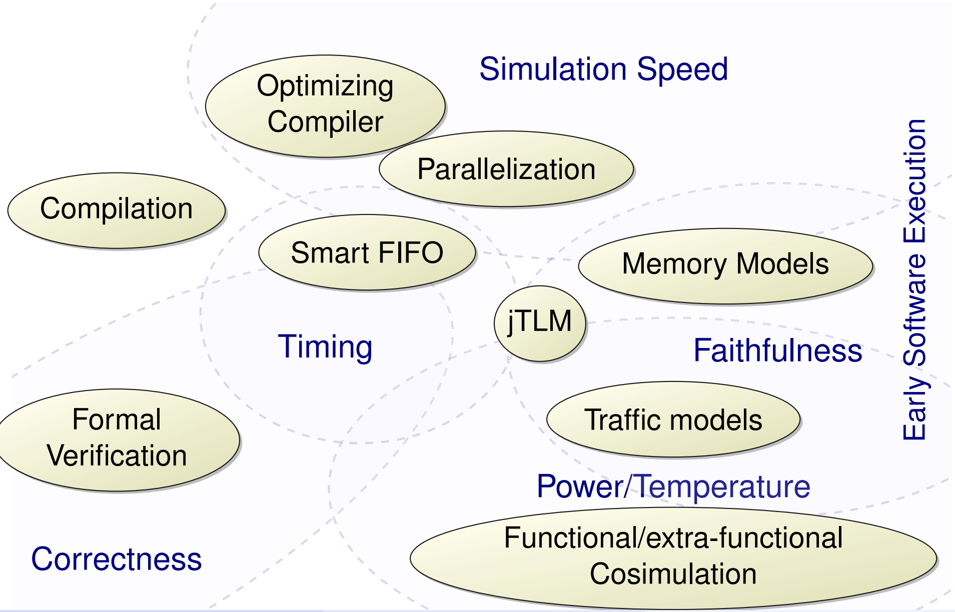

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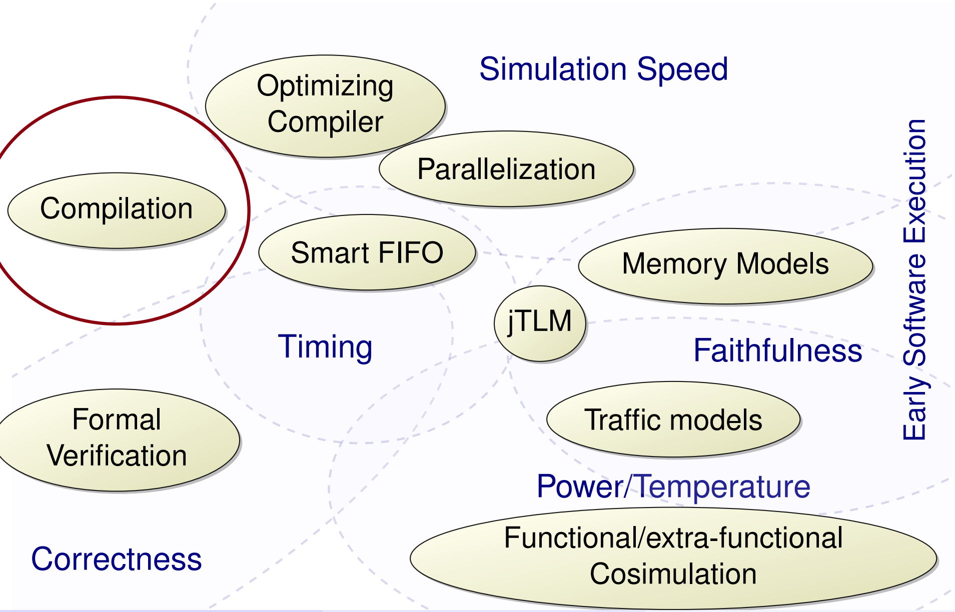
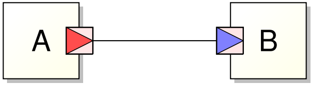


SystemC: Simple Example



```
int sc_main (int, char **) {
   /* Instanciate modules */
   A a("Alice");
   B b("Bob");

   /* Connect them together */
   a.socket.bind(b.socket);

   /* and start simulation */
   sc_start();
   return 0;
}
```

```
struct A : sc_module {
   /* Connection to outside */
   initiator_socket socket;

   /* Behavior */
   void thread() {
      do_stuff();
      write(socket, addr, data);
   }

   SC_CTOR(A) {
      SC_THREAD(thread);
   }
};
```

$\leadsto$ Compilable with any C++ compiler

Challenges and Solutions with SystemC Front-Ends

1. C++ is complex (e.g. `clang++` ≈ 400,000 LOC)

2. Architecture built at runtime, with C++ code

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Kevin Marquet

Guillaume Sergent

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   ⇝ Write a C++ front-end or reuse one (g++, clang++, EDG, . . .)
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              ther */
              ;

              n */

    return 0;
}
```

Static Approaches

```
struct A : s  module {
    /* Connect     to outside */
    initiato

    /* Be
    void
        do_st
        write(socke         data);
    }

    SC_CTOR(A) {
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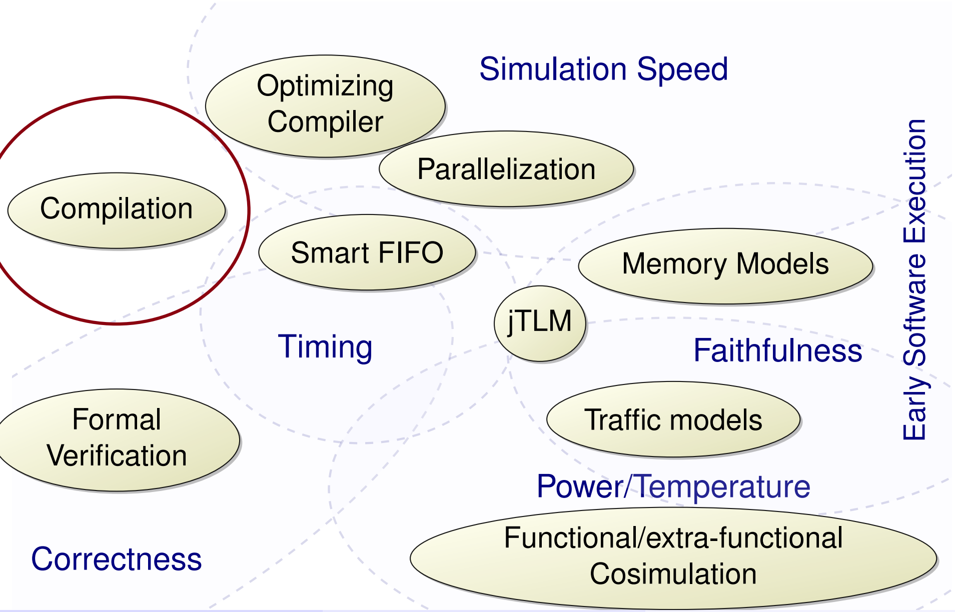
    }
};
```

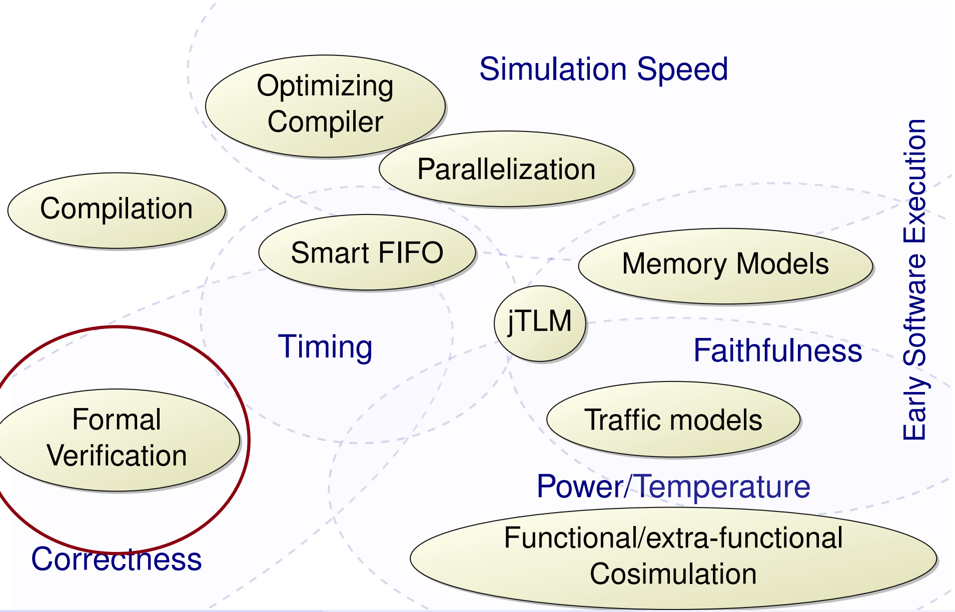
Dynamic Approaches

Kevin Marquet Guillaume Sergent

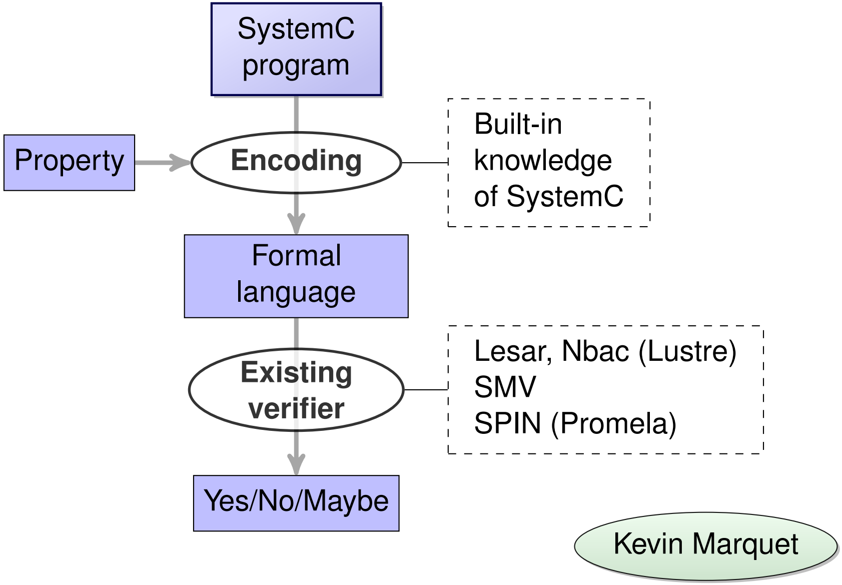
Contributions on TLM



Contributions on TLM



Formal Verification: Encoding Approaches



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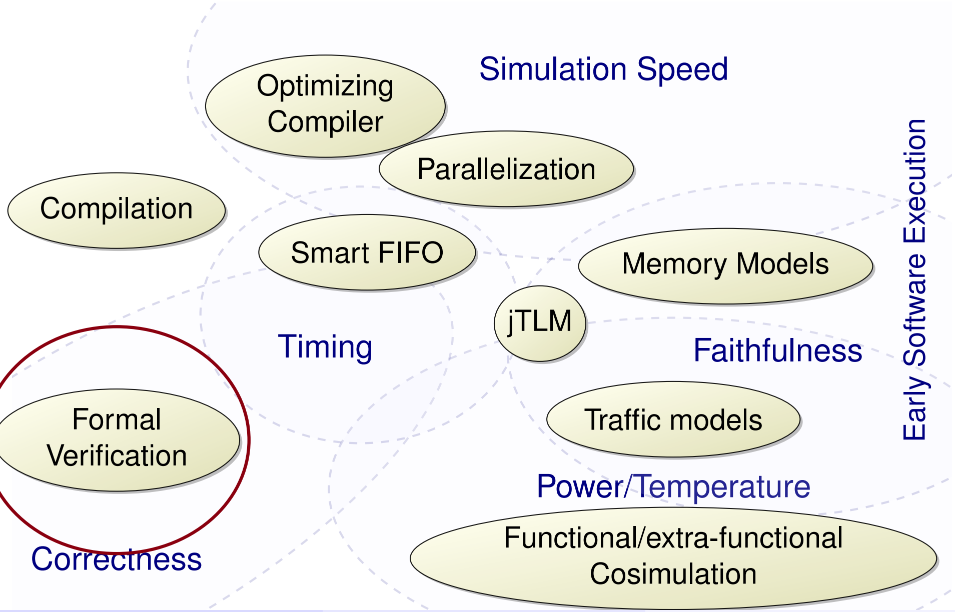

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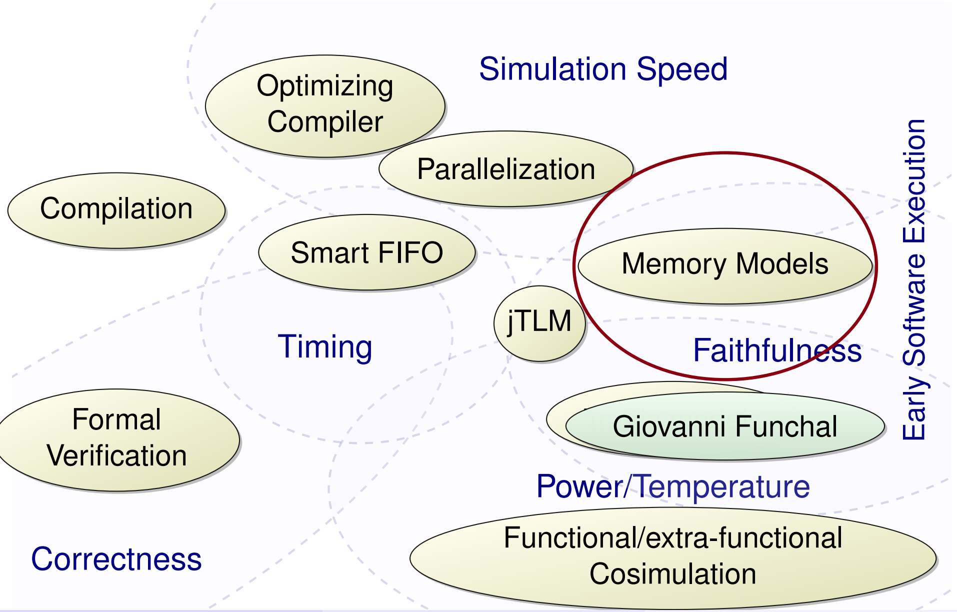

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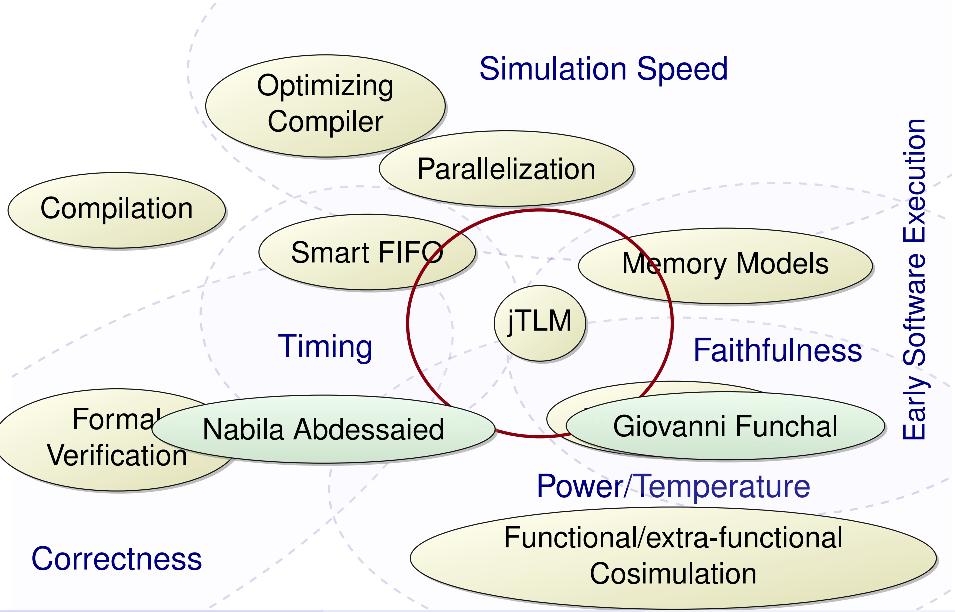

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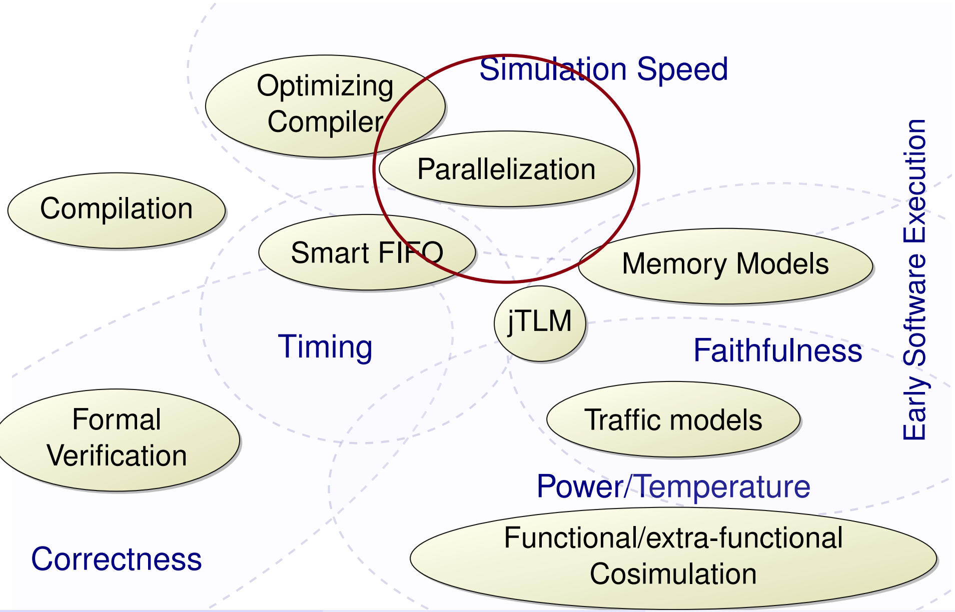
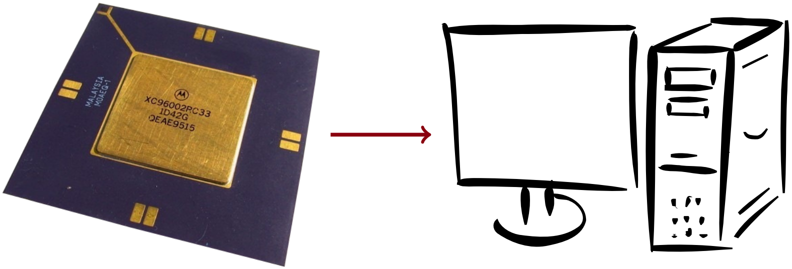
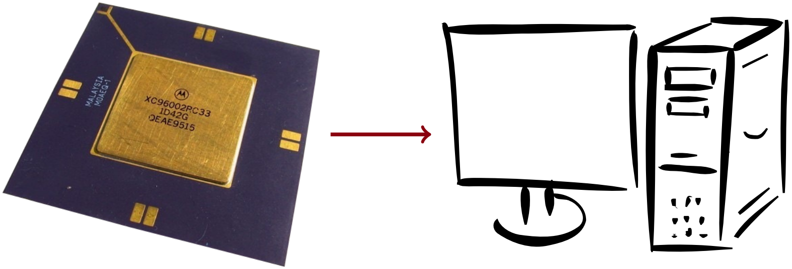


Simulation Parallelization



Simulation Parallelization



SystemC uses co-routine semantics
(Sequential)

Problems and Solutions for Parallel Execution of SystemC/TLM

(1) Execution order imposed by SystemC

(2) Race conditions (e.g. `x++` on global variable)

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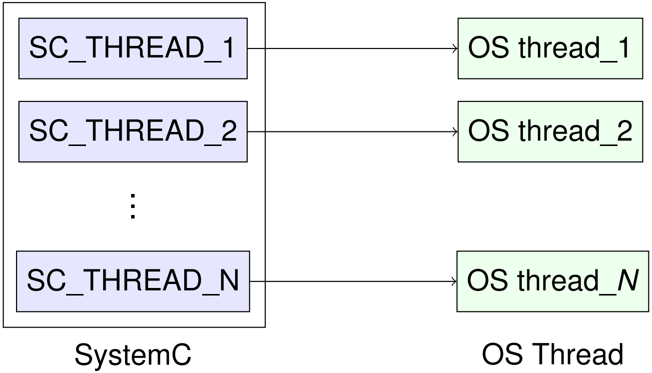
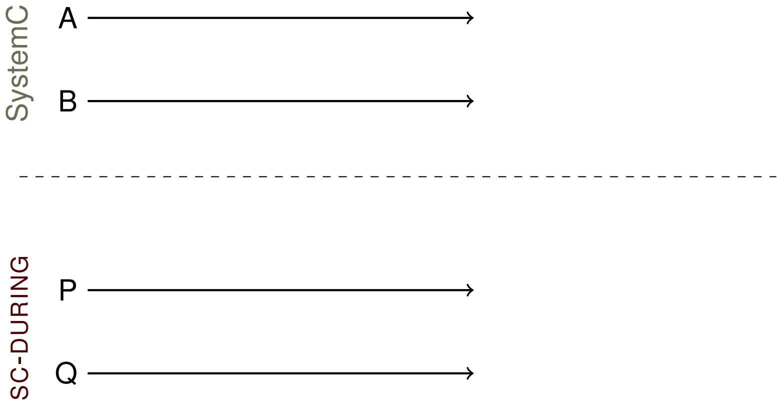
Our proposal = new constructs:
Desynchronisation (1) / Synchronisation (2)

SC-DURING: The Idea



- Unmodified SystemC
- Computations delegated to external threads
- Weak synchronization between SystemC and tasks with duration

Simulated Time in SystemC and SC-DURING



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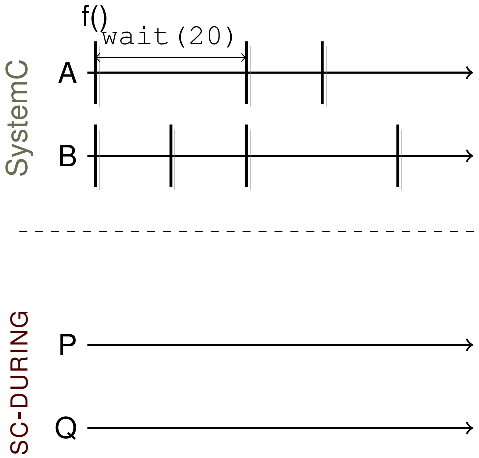
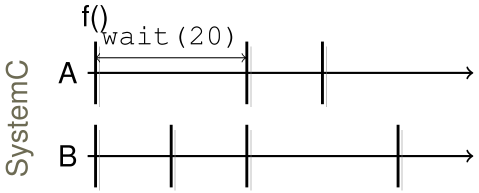


Process A:

```
//computation
f();
//time taken by f
wait(20, SC_NS);
```

Simulated Time in SystemC and SC-DURING



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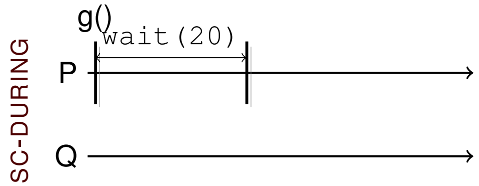
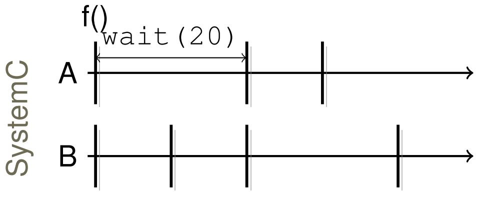


Process P:

```
g();
wait(20, SC_NS);
```

Simulated Time in SystemC and SC-DURING



Process A:

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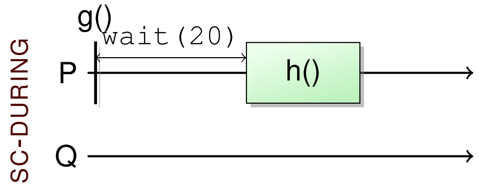

Process P:

```
g();
wait(20, SC_NS);
during(15, SC_NS, h);
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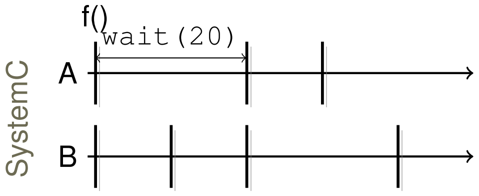
Simulated Time in SystemC and SC-DURING



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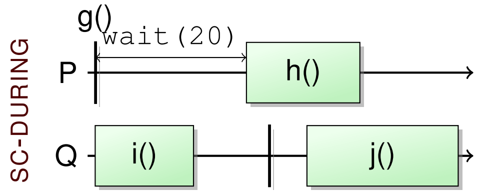
```



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SC-DURING: Sketch of Implementation

```
void during(sc_core::sc_time d,
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1   std::thread t(f); // Create thread
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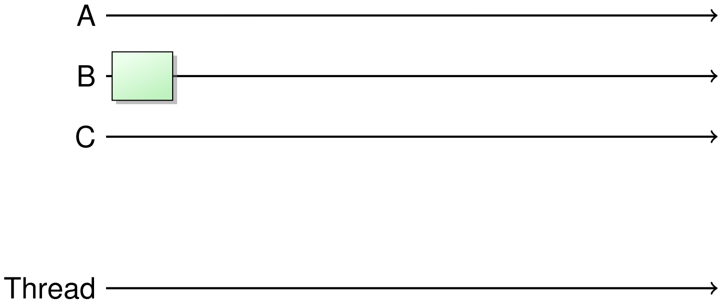
}
```



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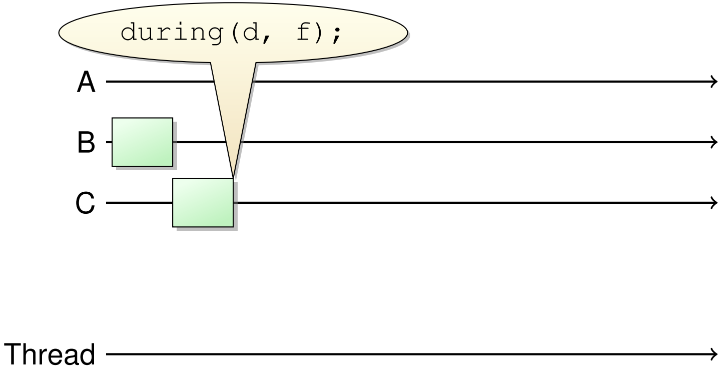

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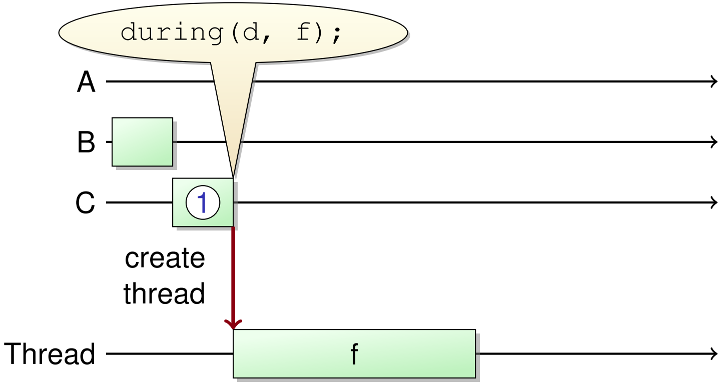
    t.join(); // Wait for completion
}
```

Markers 1, 2, 3 stand beside the three lines of the function body.



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```
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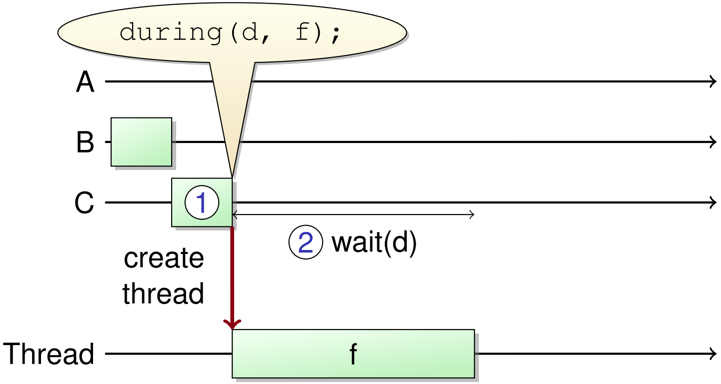

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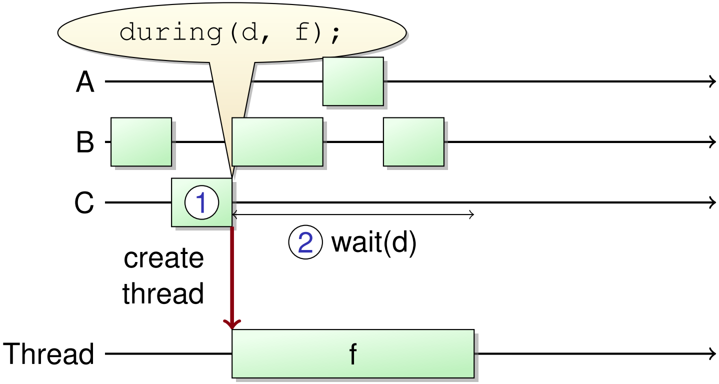

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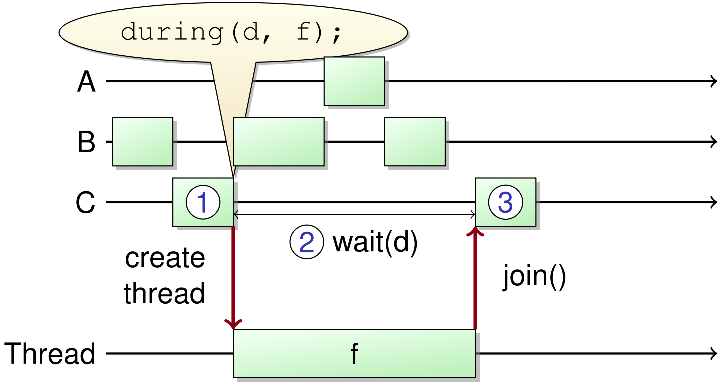

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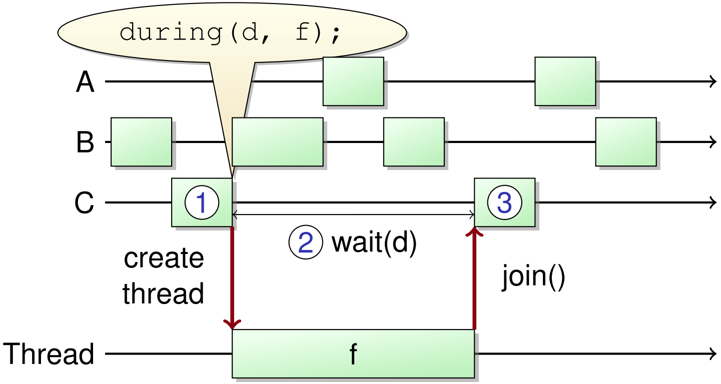

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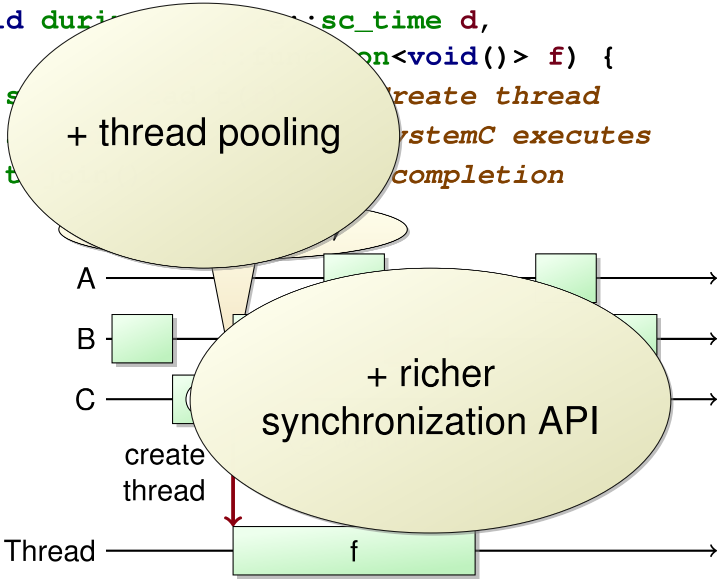
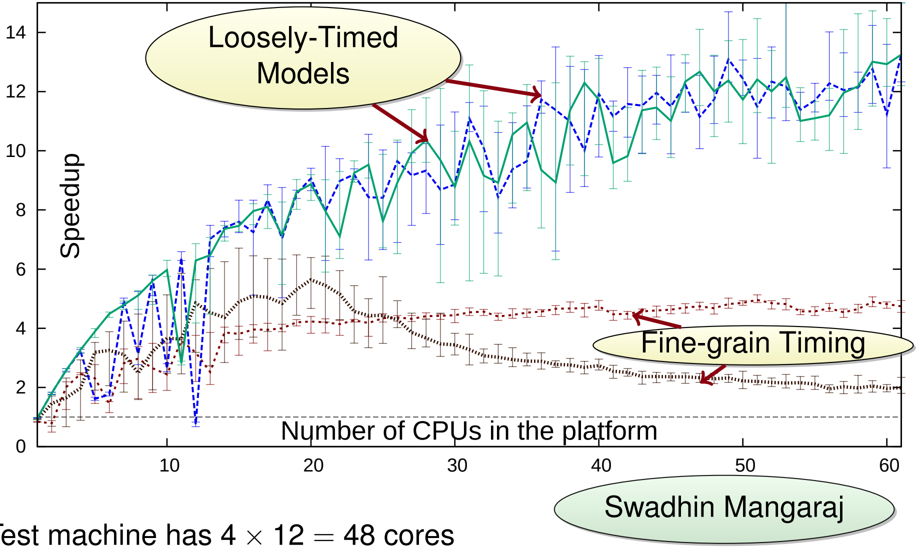
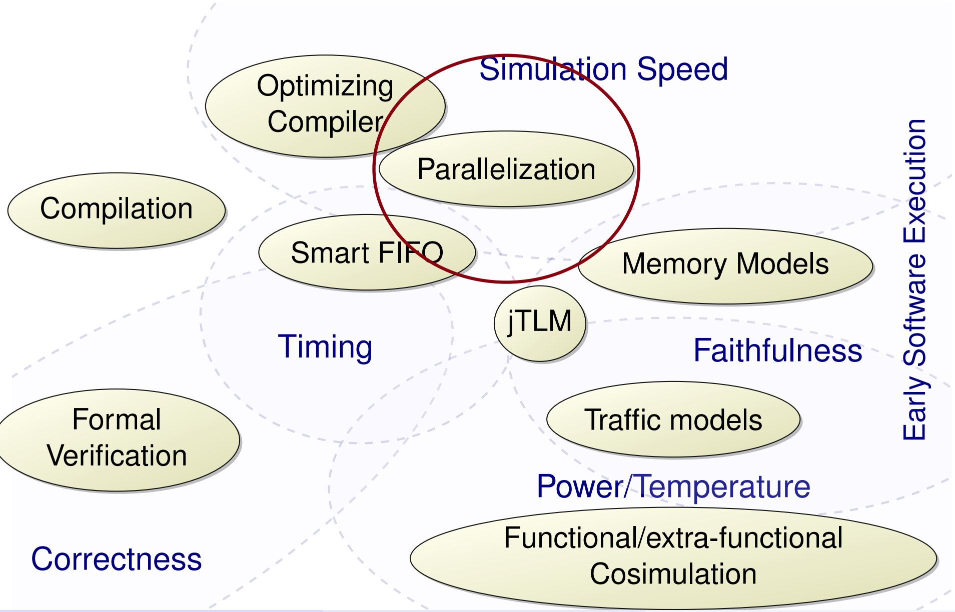


SC-DURING: Results



Test machine has $4 \times 12 = 48$ cores

Contributions on TLM



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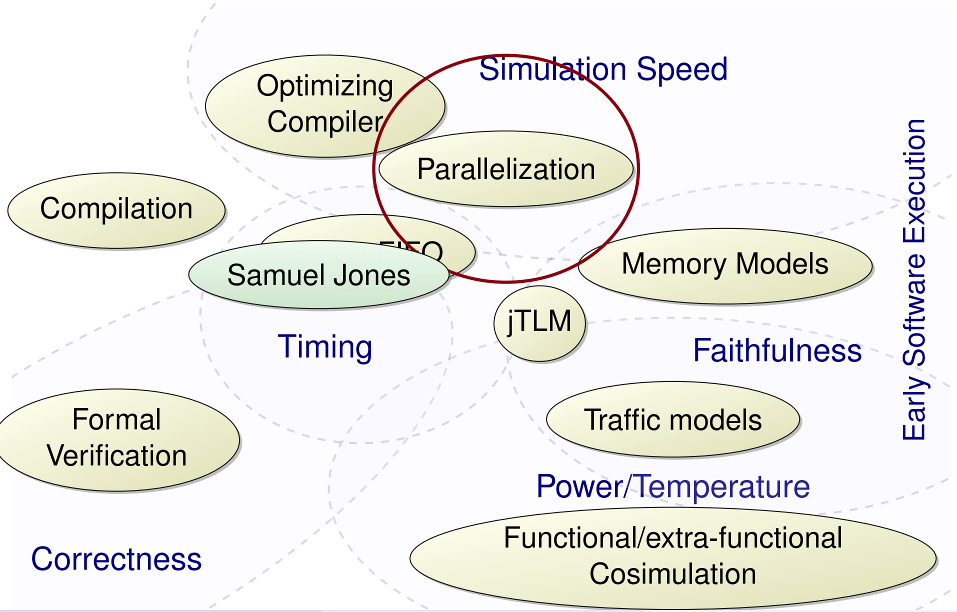

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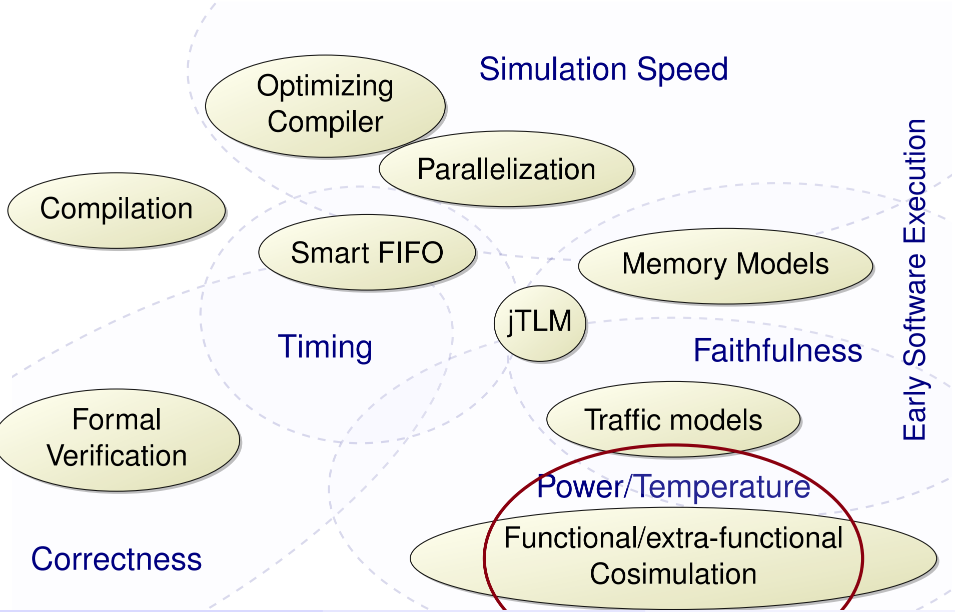
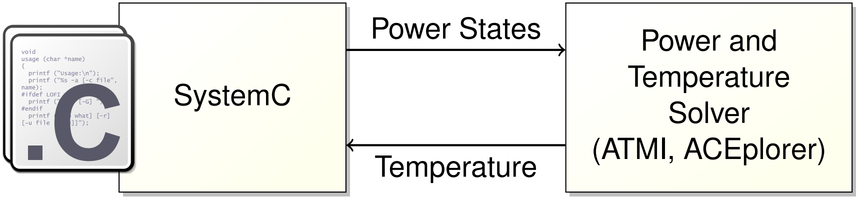


SystemC and Extra-Functional Solver Cosimulation



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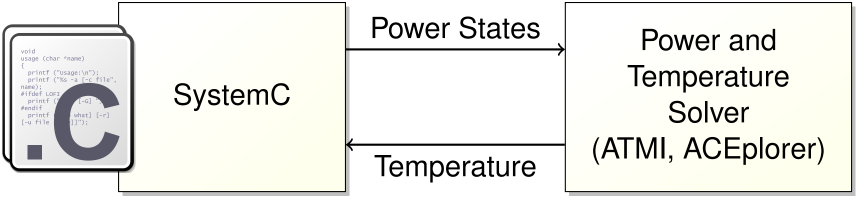
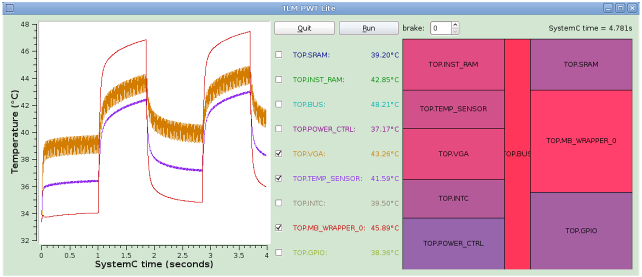


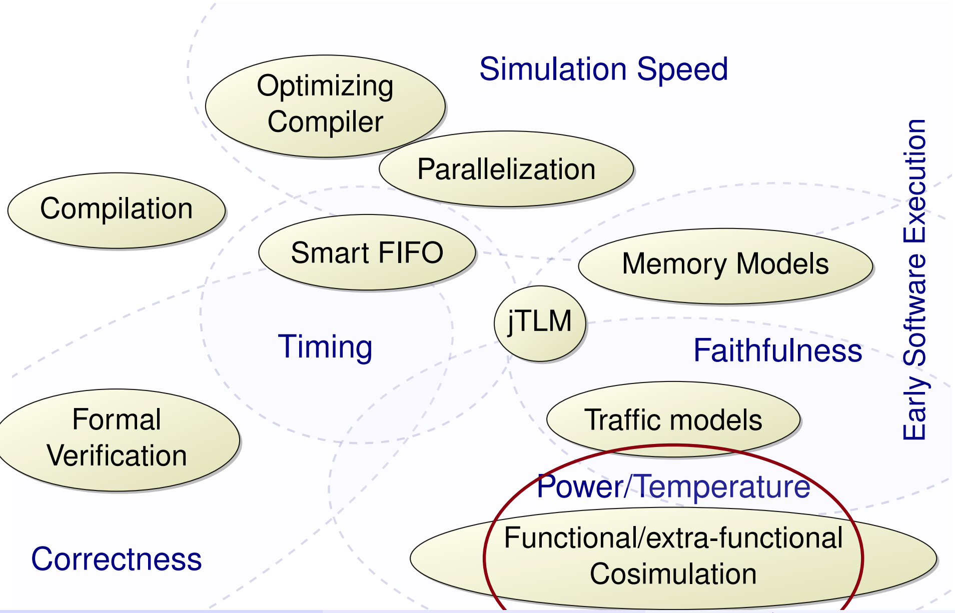

TLM PWT Lite

Quit   Run   brake: 0   SystemC time = 4.781s

- [ ] TOP.SRAM: 39.20°C
- [ ] TOP.INST_RAM: 42.85°C
- [ ] TOP.BUS: 48.21°C
- [ ] TOP.POWER_CTRL: 37.17°C
- [x] TOP.VGA: 43.26°C
- [x] TOP.TEMP_SENSOR: 41.59°C
- [ ] TOP.INTC: 39.50°C
- [x] TOP.MB_WRAPPER_0: 45.89°C
- [ ] TOP.GPIO: 38.36°C

Claude Helmstetter   Tayeb Bouhadiba

Contributions on TLM



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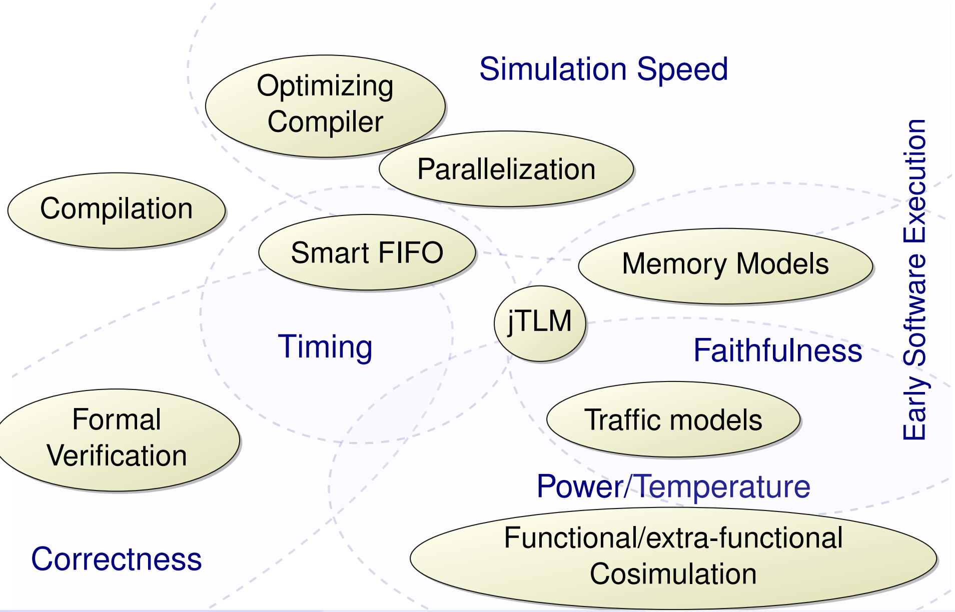
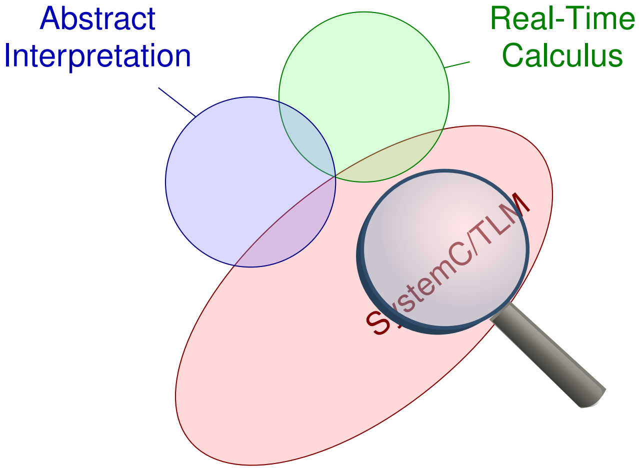


Outline



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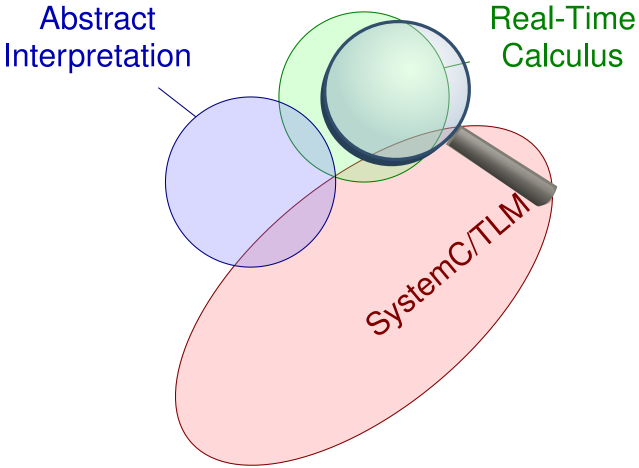
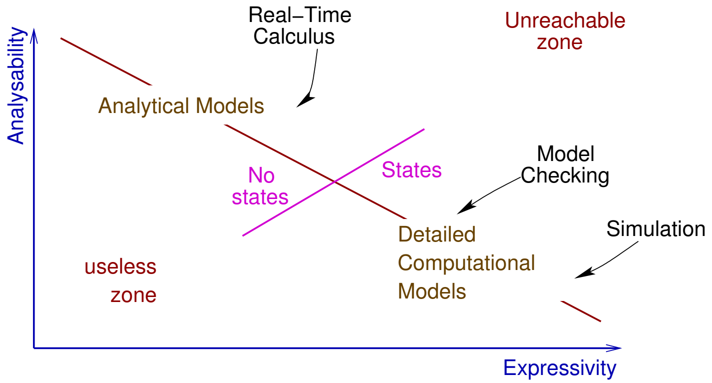
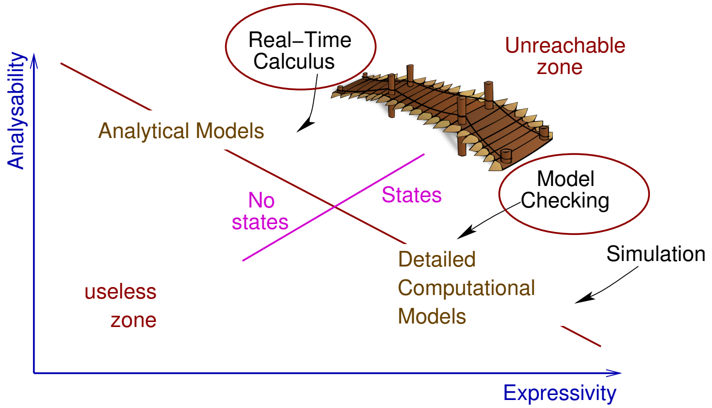


Precision Vs Algorithmic Complexity

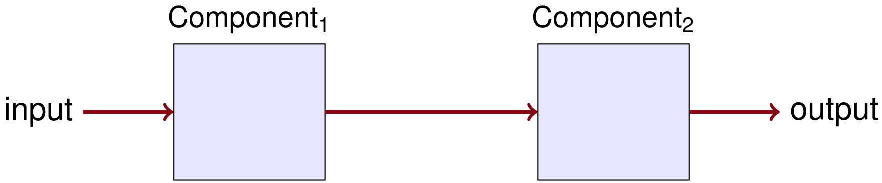


Precision Vs Algorithmic Complexity



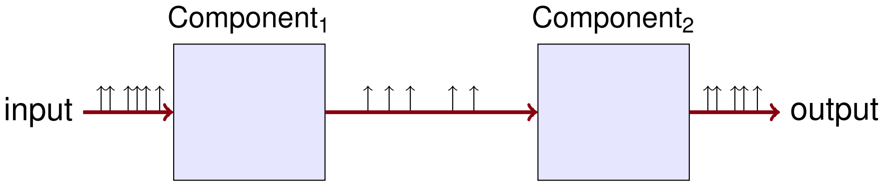
Modular Performance Analysis (MPA): The Big Picture

[Thiele et al.]



Modular Performance Analysis (MPA): The Big Picture

[Thiele et al.]



Modular Performance Analysis (MPA): The Big Picture

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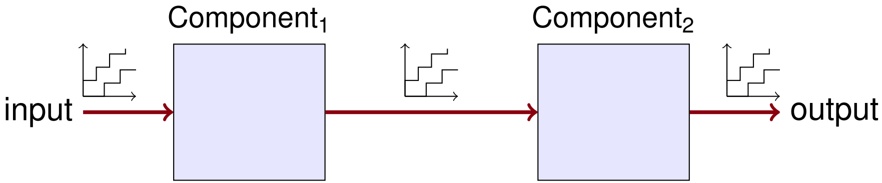

Modular Performance Analysis (MPA): The Big Picture

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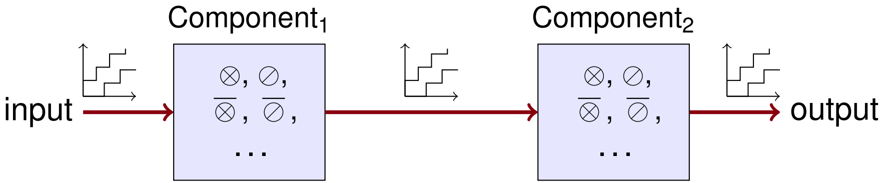
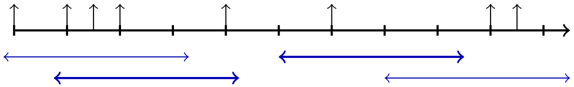
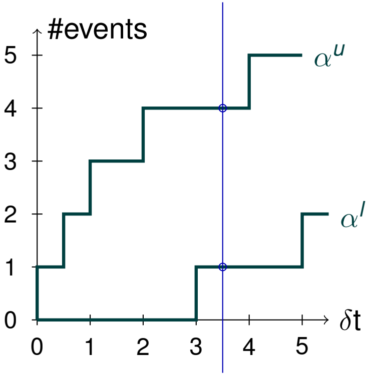


Real-Time Calculus and Arrival Curves

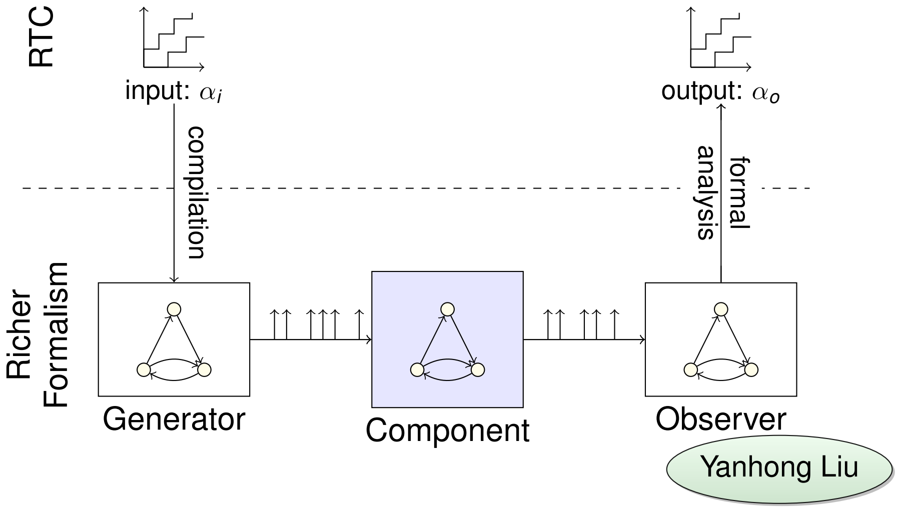




$\alpha^u(t)$ / $\alpha^l(t)$: min/max number of events in any window of duration t.

Interfacing with Timed Automata

[Chakraborty et al.]

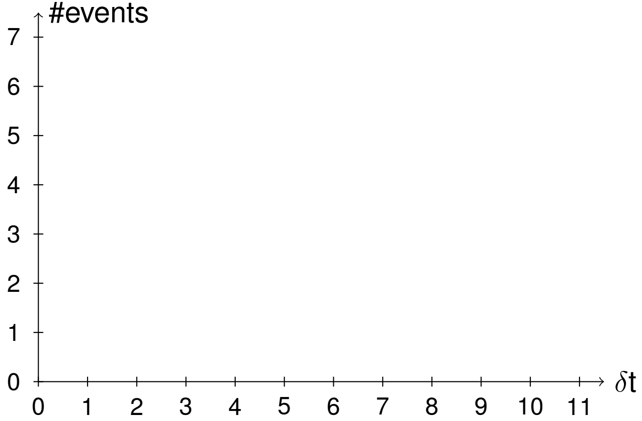


Timed Automata Vs Abstract Interpretation and SMT-Solving

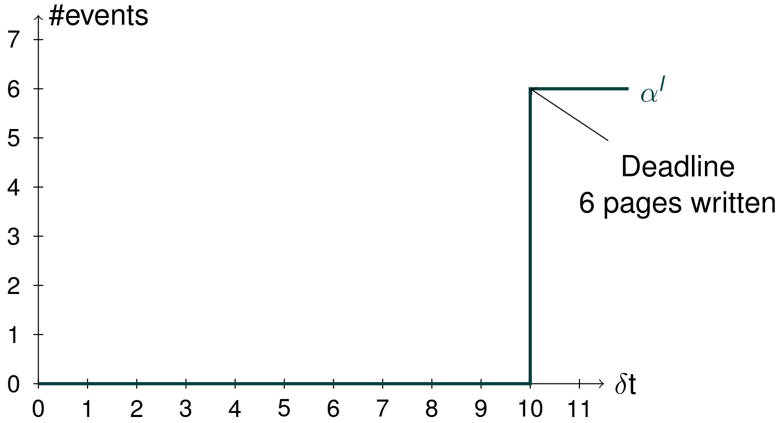
	Large event counters	Large timing constants
Timed automata (Uppaal)	💣	🍰
SMT solving	🍰	💣
Abstract Interpretation	🍰	💣

ac2lus: use Lustre tools to analyze MPA components
(Nbac = abstract interpretation, Kind = SMT solving)

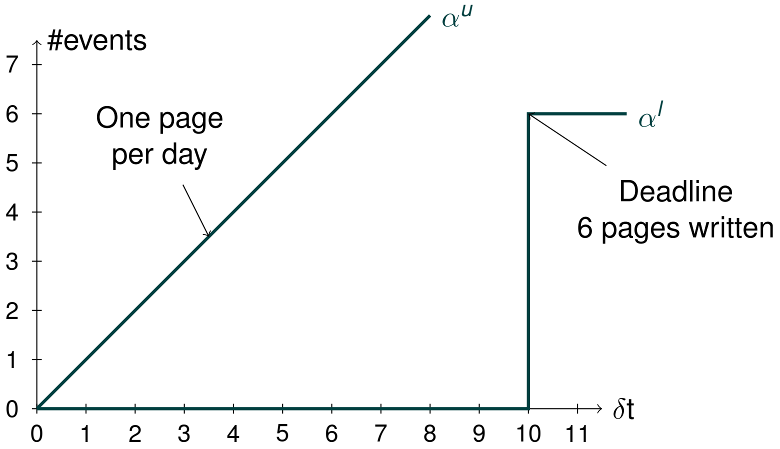
The Causality Problem



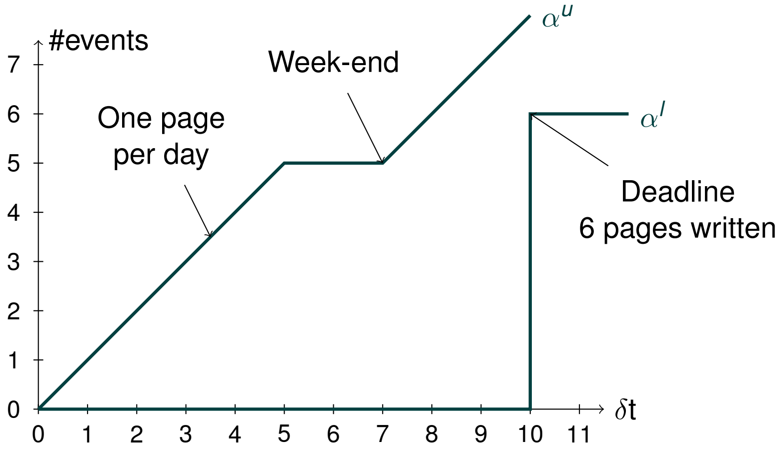
The Causality Problem



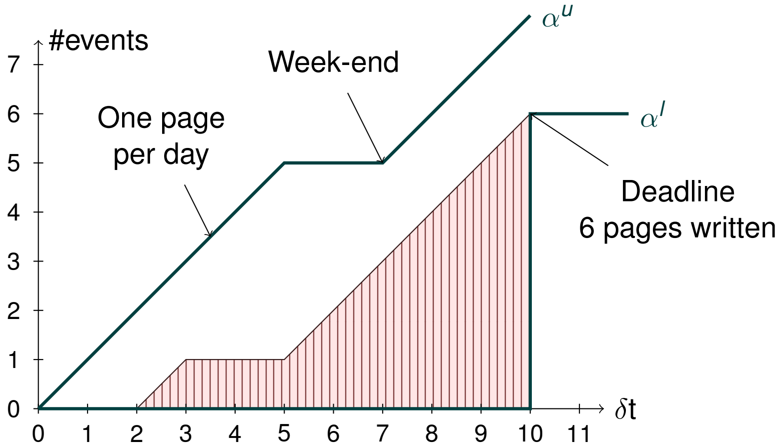
The Causality Problem



The Causality Problem

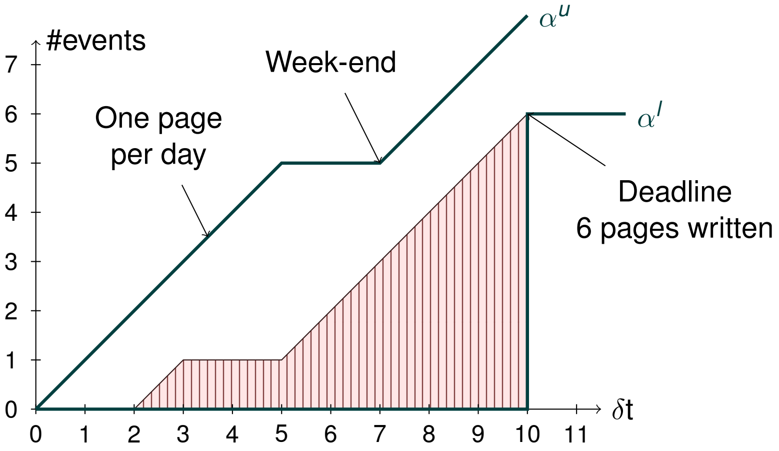


The Causality Problem



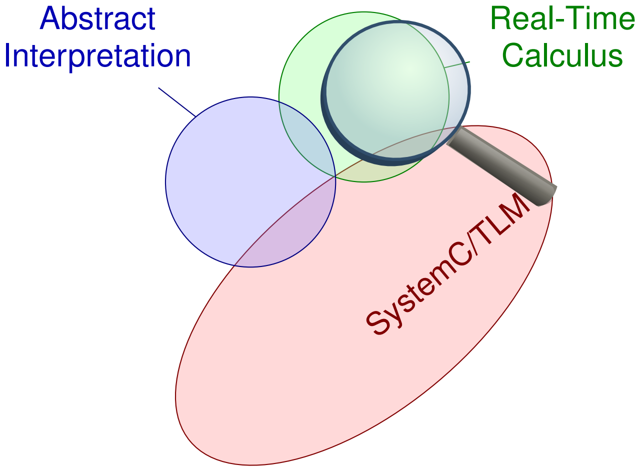
Implicit constraint: maximal procrastination = 2 days

The Causality Problem



Causality closure = compute the implicit constraint automatically

Outline



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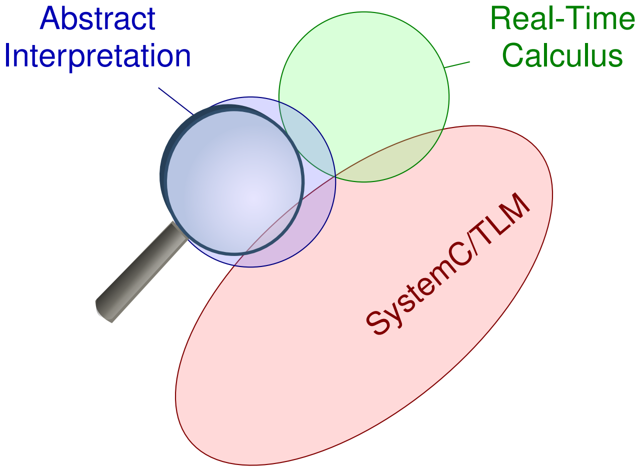


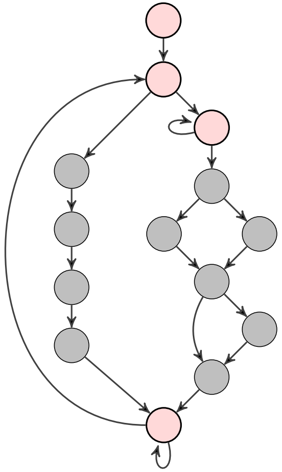
Abstract Interpretation and PAGAI

```
$ pagai -i test.c
void f() {
        int x = 0, y = 1;
        /* invariant:
           y = x + 1
           y <= 102
           y >= 1
        */
        while (x <= 100) {
                x++;
                y++;
        }
}
```

Julien Henry

Abstract Interpretation with PAGAI

[Cousot & Cousot]



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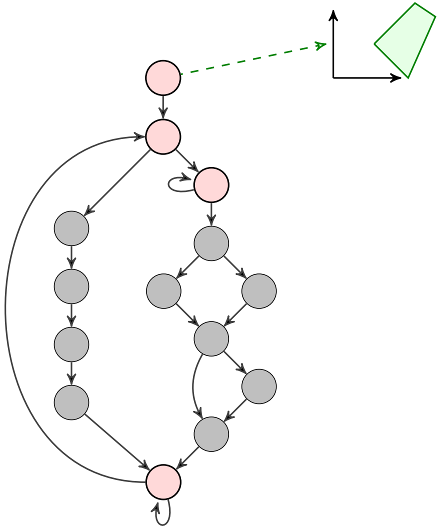

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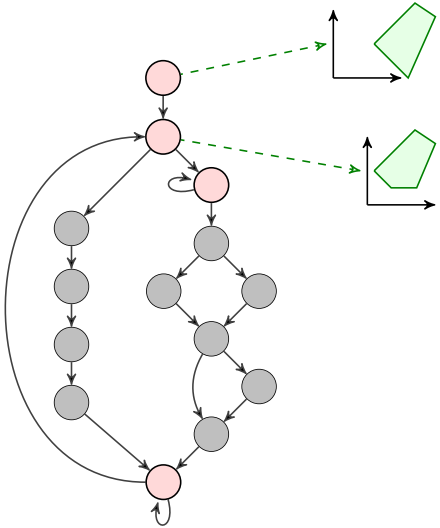

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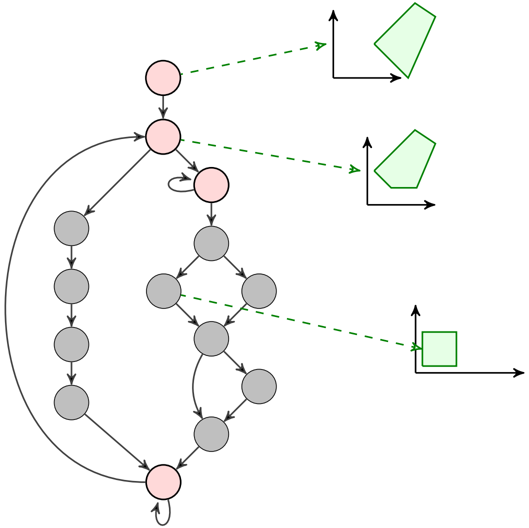

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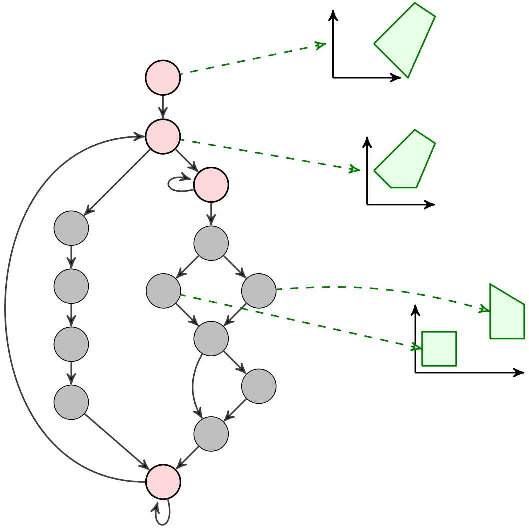

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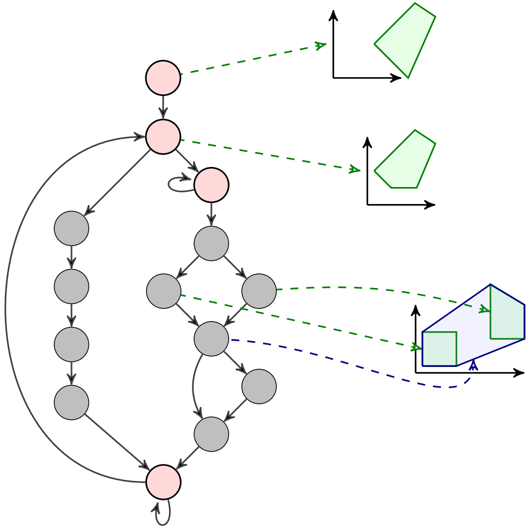
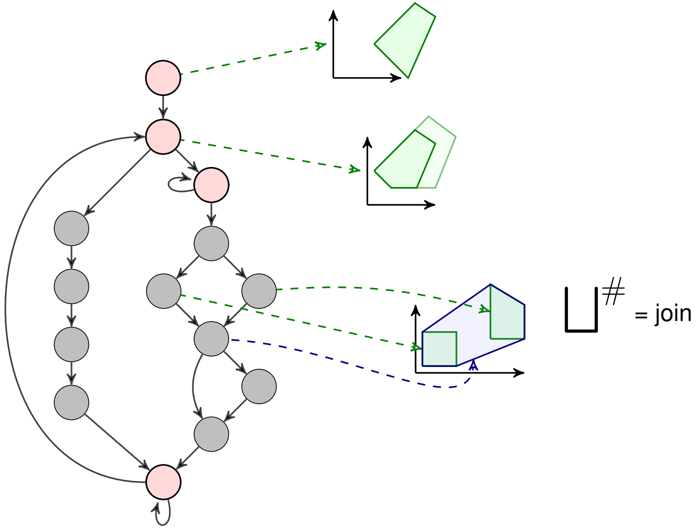


$\bigsqcup^{\#}$ = join

Abstract Interpretation with PAGAI

[Cousot & Cousot]



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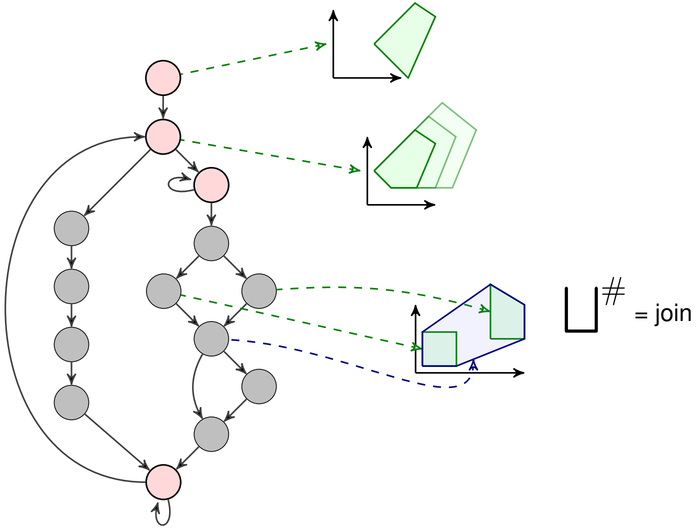

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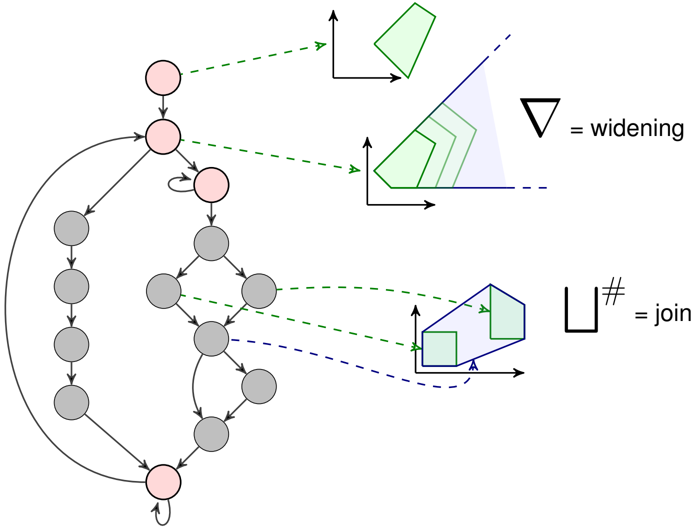

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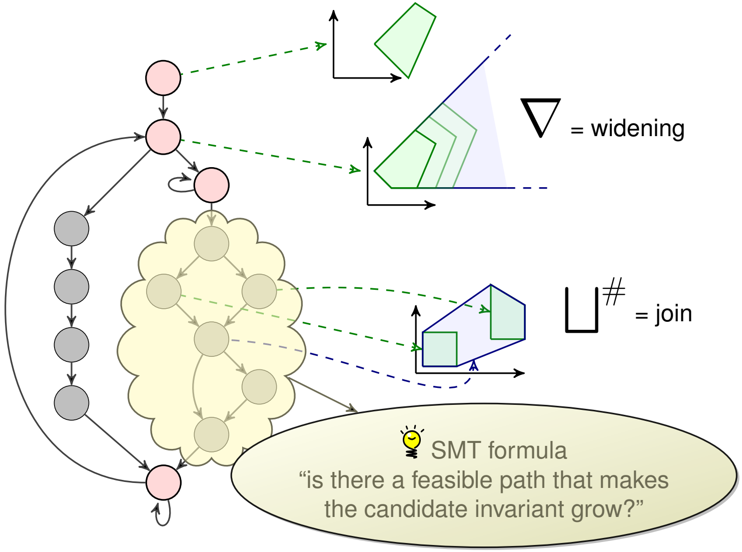
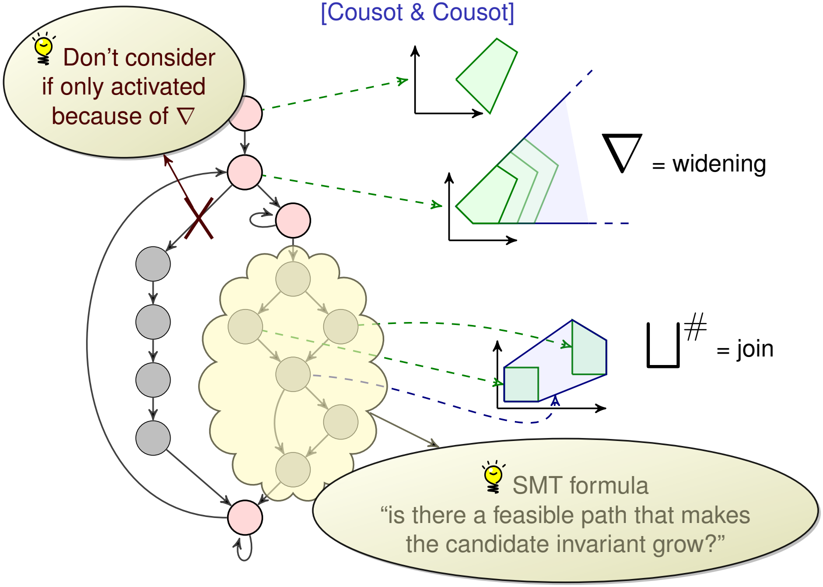


SMT formula
"is there a feasible path that makes the candidate invariant grow?"

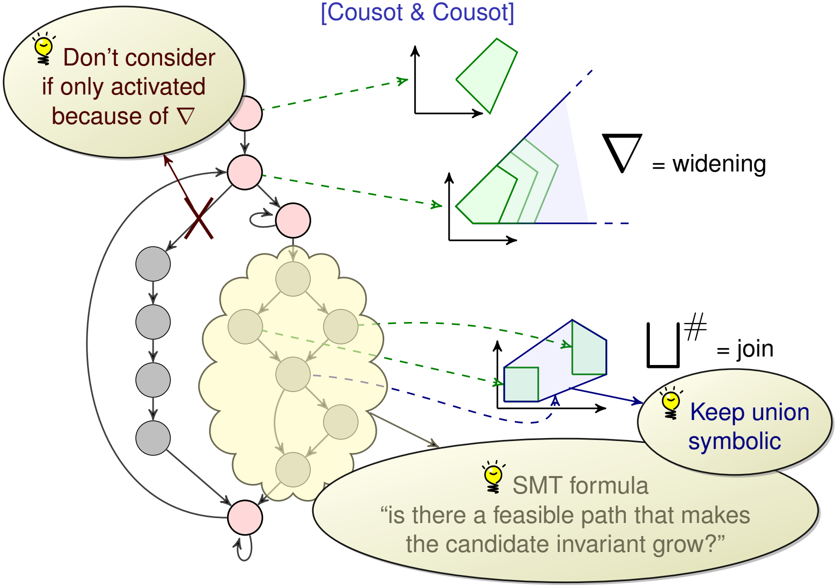
Abstract Interpretation with PAGAI

[Cousot & Cousot]


Don't consider if only activated because of ∇
∇ = widening
$\sqcup^\#$ = join
SMT formula "is there a feasible path that makes the candidate invariant grow?"

Abstract Interpretation with PAGAI

[Cousot & Cousot]

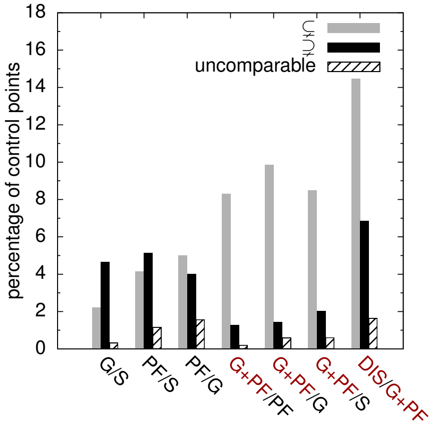

Don't consider if only activated because of ∇
∇ = widening
$\bigsqcup^{\#}$ = join
Keep union symbolic
SMT formula
"is there a feasible path that makes the candidate invariant grow?"

PAGAI: Results

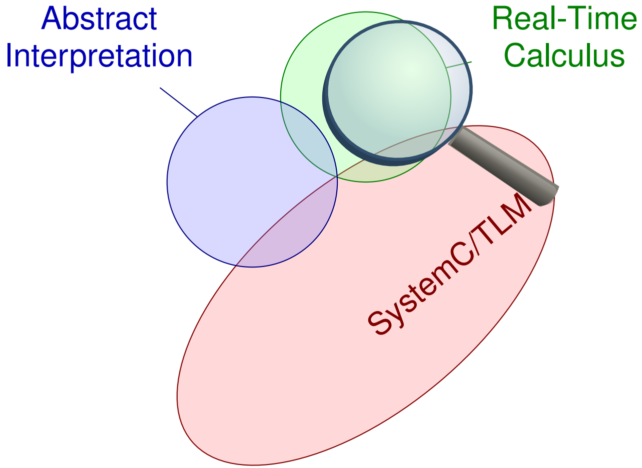
Tested on real programs

Name	kLOC	|*loops*|	Time (in seconds) S	G	PF	C	DIS
a2ps	55	2012	23	74	34	115	162
gawk	59	902	15	46	12	40	50
gnuchess	38	1222	50	220	81	312	351
gnugo	83	2801	77	159	92	766	1493
grep	35	820	41	85	22	65	122
gzip	27	494	22	268	91	303	230
lapack	954	16422	294	3740	3773	8159	10351
make	34	993	67	108	53	109	257
tar	73	1712	37	218	115	253	396

Improves discovered invariants



Outline



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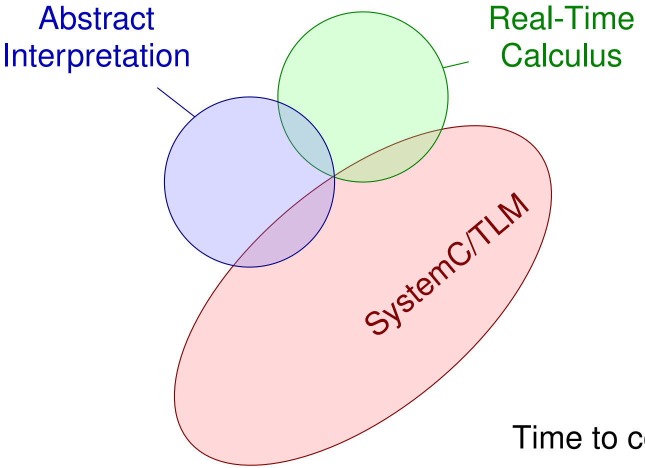
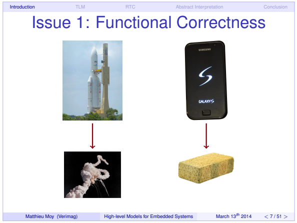


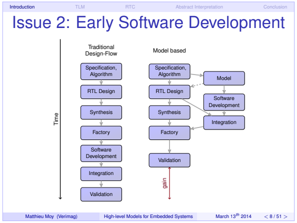
Time to conclude...

Summary


Introduction TLM RTC Abstract Interpretation Conclusion

Issue 1: Functional Correctness

Matthieu Moy (Verimag) High-level Models for Embedded Systems March 13th 2014 < 7 / 51 >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Issue 2: Early Software Development

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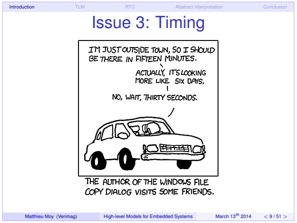
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Issue 3: Timing

I'M JUST OUTSIDE TOWN, SO I SHOULD BE THERE IN FIFTEEN MINUTES.
ACTUALLY, IT'S LOOKING MORE LIKE SIX DAYS.
NO, WAIT, THIRTY SECONDS.

THE AUTHOR OF THE WINDOWS FILE COPY DIALOG VISITS SOME FRIENDS.

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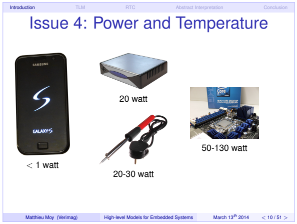
Introduction TLM RTC Abstract Interpretation Conclusion

Issue 4: Power and Temperature

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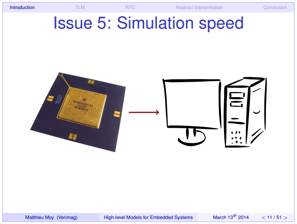
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Issue 5: Simulation speed

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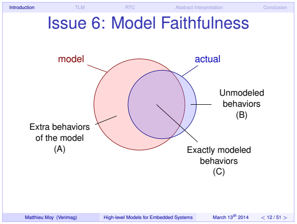
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Issue 6: Model Faithfulness

model
actual
Unmodeled behaviors (B)
Extra behaviors of the model (A)
Exactly modeled behaviors (C)

Matthieu Moy (Verimag) High-level Models for Embedded Systems March 13th 2014 < 12 / 51 >

Scientific Production

Software Pinapa, PinaVM, PAGAI, LIBTLMPWT, SC-DURING, ac2lus, ...

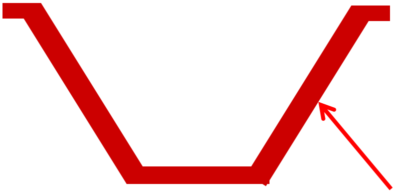
Papers 15 international conferences, 9 workshops, 1 book chapter, 1 journal.

Trained students

- Completed: 1 Ph.D, 5 research master, 6 post-docs, 20 short internships
- Ongoing: 2 Ph.D, 2 research master, 3 short internships

Ensimag course on SystemC/TLM

Condition for Success of a Lab/Industry Cooperation

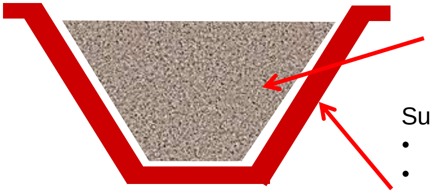


Suitable environment:

- Shared motivation
- Understanding and respect of each party's constraints
- Legal framework
- Bonus: geographic proximity

(Slide from Laurent Maillet-Contoz)

Condition for Success of a Lab/Industry Cooperation



A common ground
- Scientific context
- Applicative context

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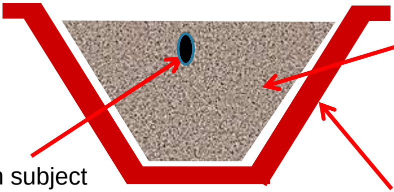

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A research subject covering shared interests

life.augmented

(Slide from Laurent Maillet-Contoz)

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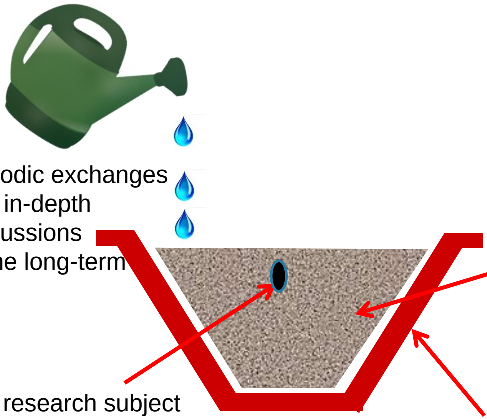

Periodic exchanges and in-depth discussions

In the long-term

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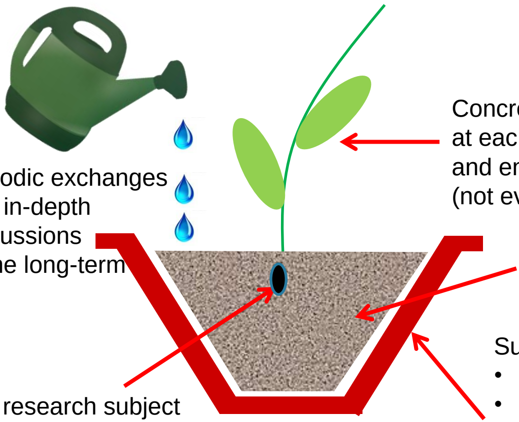

Concrete works to progress at each party’s own rythm and enrich the landscape (not everything will succeed)

Periodic exchanges and in-depth discussions
In the long-term

A common ground
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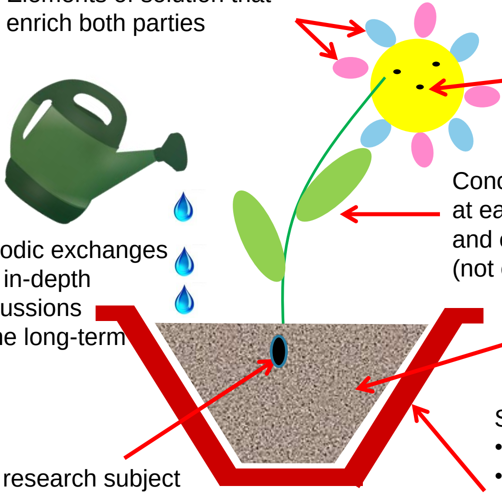
(Slide from Laurent Maillet-Contoz)

Condition for Success of a Lab/Industry Cooperation



Elements of solution that enrich both parties

Next cooperation theme

Concrete works to progress at each party's own rythm and enrich the landscape (not everything will succeed)

Periodic exchanges and in-depth discussions In the long-term

A common ground
- Scientific context
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Suitable environment:
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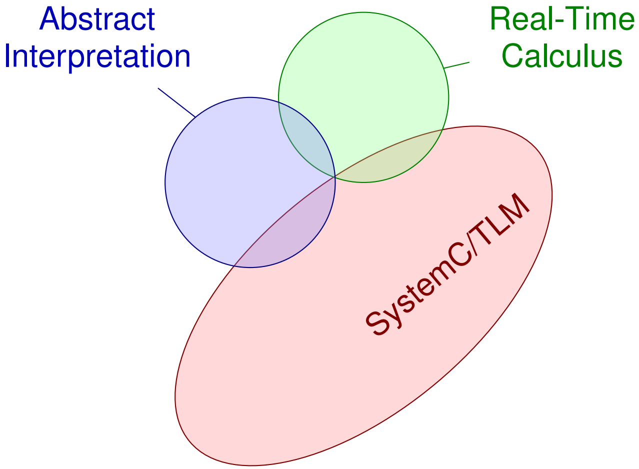
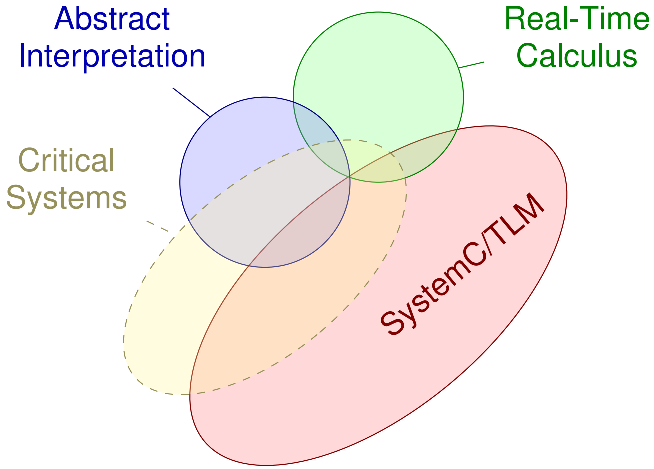
(Slide from Laurent Maillet-Contoz)

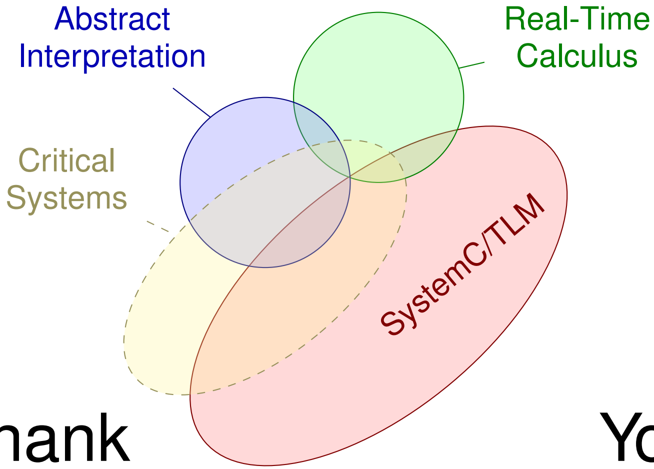
Prospects



Prospects


Abstract Interpretation
Real-Time Calculus
Critical Systems
SystemC/TLM

Questions?

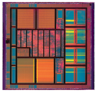


Thank You!

Supervised/Co-supervised Ph.D

Giovanni Funchal	2007 $\rightarrow$ 2011 CIFRE STMicroelectronics co-supervised with Florence Maraninchi
Julien Henry	2011 $\rightarrow$ present co-supervised with David Monniaux
Swadhin Mangaraj	2013 $\rightarrow$ present OpenES european project

Sources



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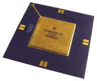

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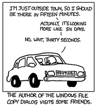
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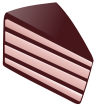

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