Formal and Informal Methods for Multi-Core Design Space Exploration

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Context

Minalogic project ATHOLE

- Low-power multi-processors platform for embedded systems.
- Partners: STMicroelectronics, CEA Leti, Thales, CWS, Verimag.
- Verimag: High level modeling and analysis.

Contribution

- Development of a framework for modeling and analysis of embedded systems.

Motivation

Embedded Systems Design

- Several design choices both in hardware and software

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- Each has advantages according to different criteria:
  - Timing performance
  - Power consumption
  - Platform cost
  - ...

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Needs

- **Performance estimation as soon as possible**
  - evaluate quickly different trade-offs
- Exploration and Analysis on a high level of abstraction.

Verimag

High-Level Performance Evaluation

Advantage

- Works at virtual level:
  - No need for a physical platform
  - No need for a complete implementation
- Models are simplified:
  - Performance analysis is tractable
  - Simulation and analysis are fast
- Evaluation of different alternatives can be done easily

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To compensate the lack of precision at this level of description:

- Increase the uncertainty margins
- Consider this uncertainty in the analysis

Uncertainty

Modeling uncertainty with timed automata

- Timing informations are modeled as intervals
- Exhaustive reachability analysis
- Analysis is **worst-case oriented** and sometimes intractable.

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Modeling uncertainty probabilistically

- Duration Probabilistic Automata:
  - Timed automata with probabilistic durations
  - Discrete event simulation and statistical analysis
  - *Exact computation of expected termination time*

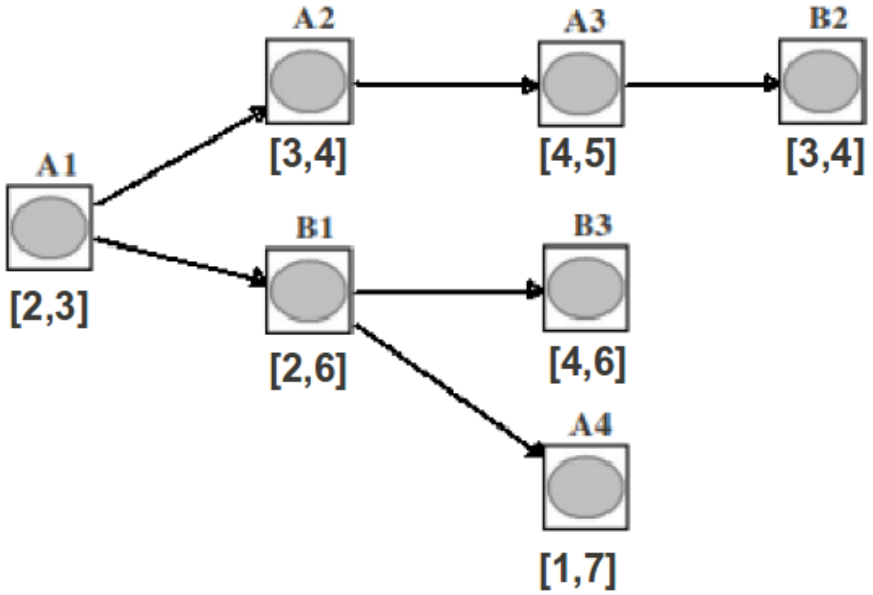
A motivating example

We show, with this example, the importance of considering the *uncertainty* in the analysis.

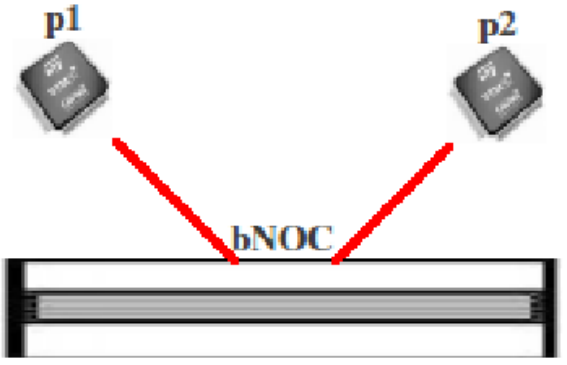
Outcome

- Timing analysis based exclusively on **worst case execution times** might not catch the **worst behavior**

Abstract Model

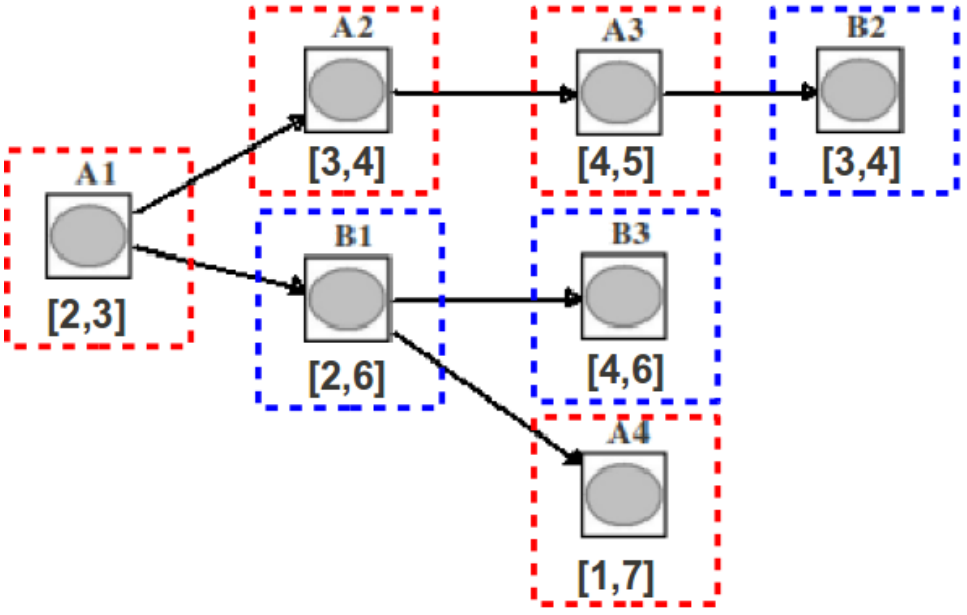


Task Graph



Architecture

Abstract Model



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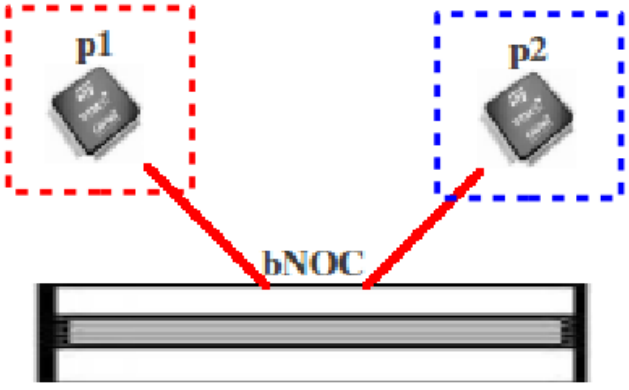

Architecture

- FIFO scheduling (non preemptive)

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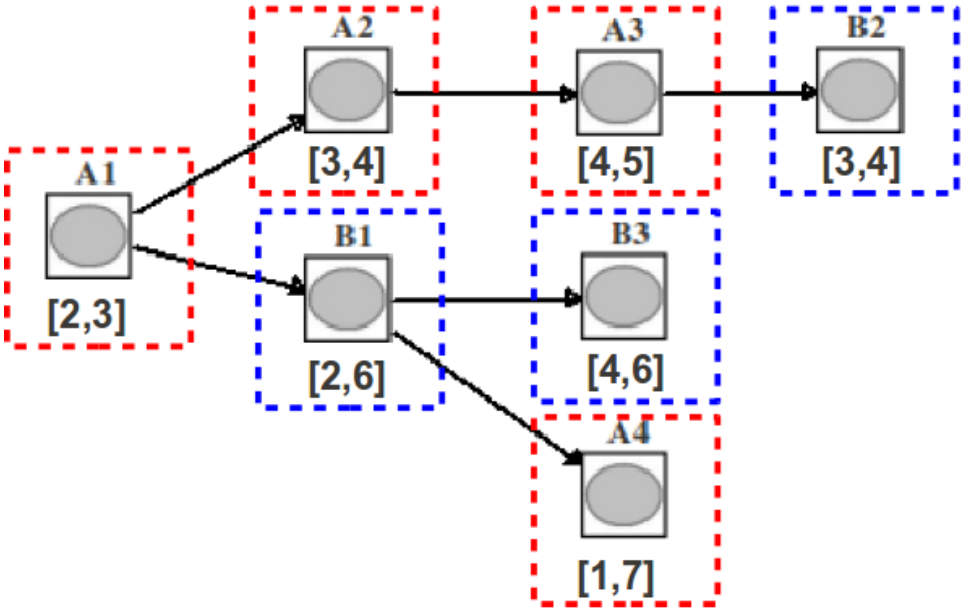

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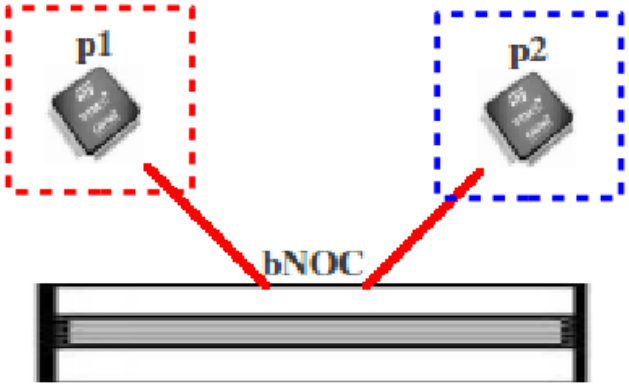

Architecture

- FIFO scheduling (non preemptive)
- Question:
  - **What is the maximal response time of the job ?**

Corner-Case Analysis

- Naively, to get the maximal response time, one might do an analysis based on *worst-case execution time* for all tasks.

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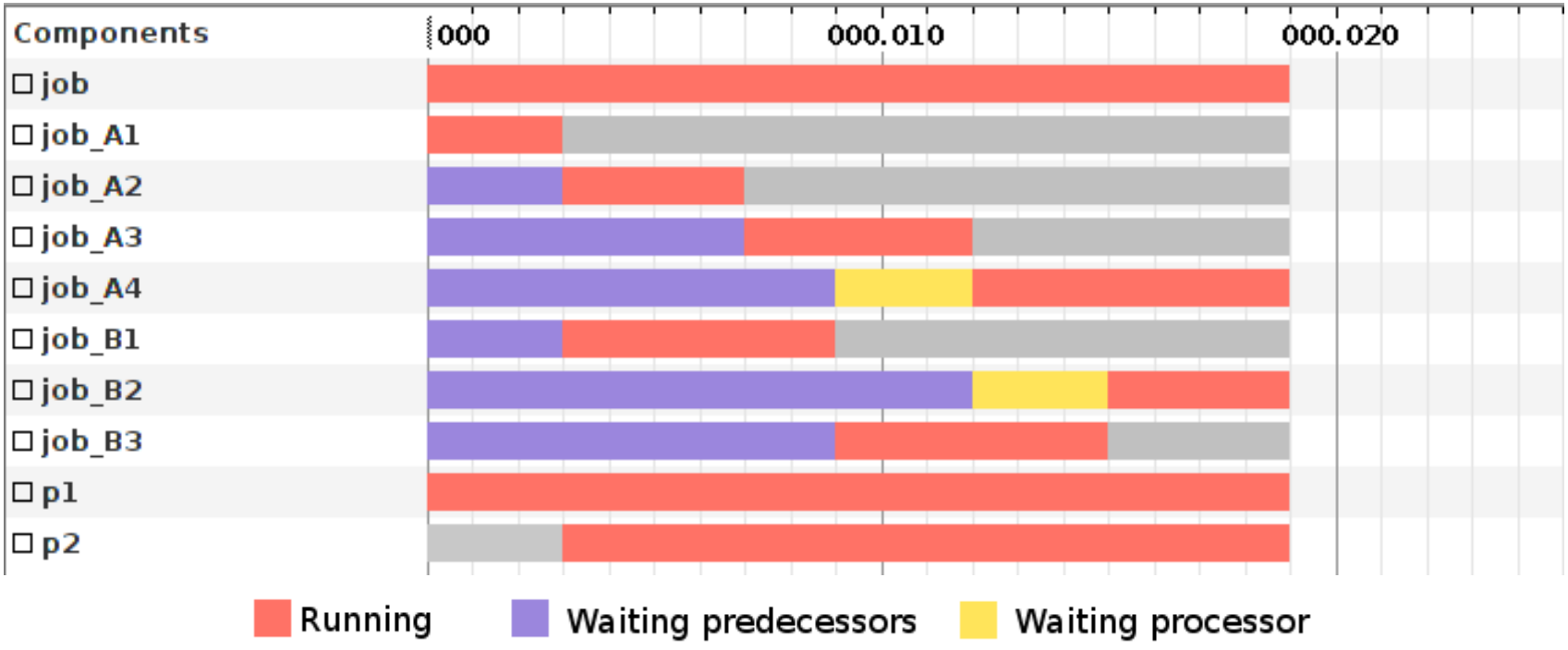

- Analysis gives a response time of 19 timeunits

Reachability Analysis with Uncertainty

We use now timed automata reachability analysis:

- Explore all possible behaviors.
- Retrieve the execution trace leading to the worst response time.

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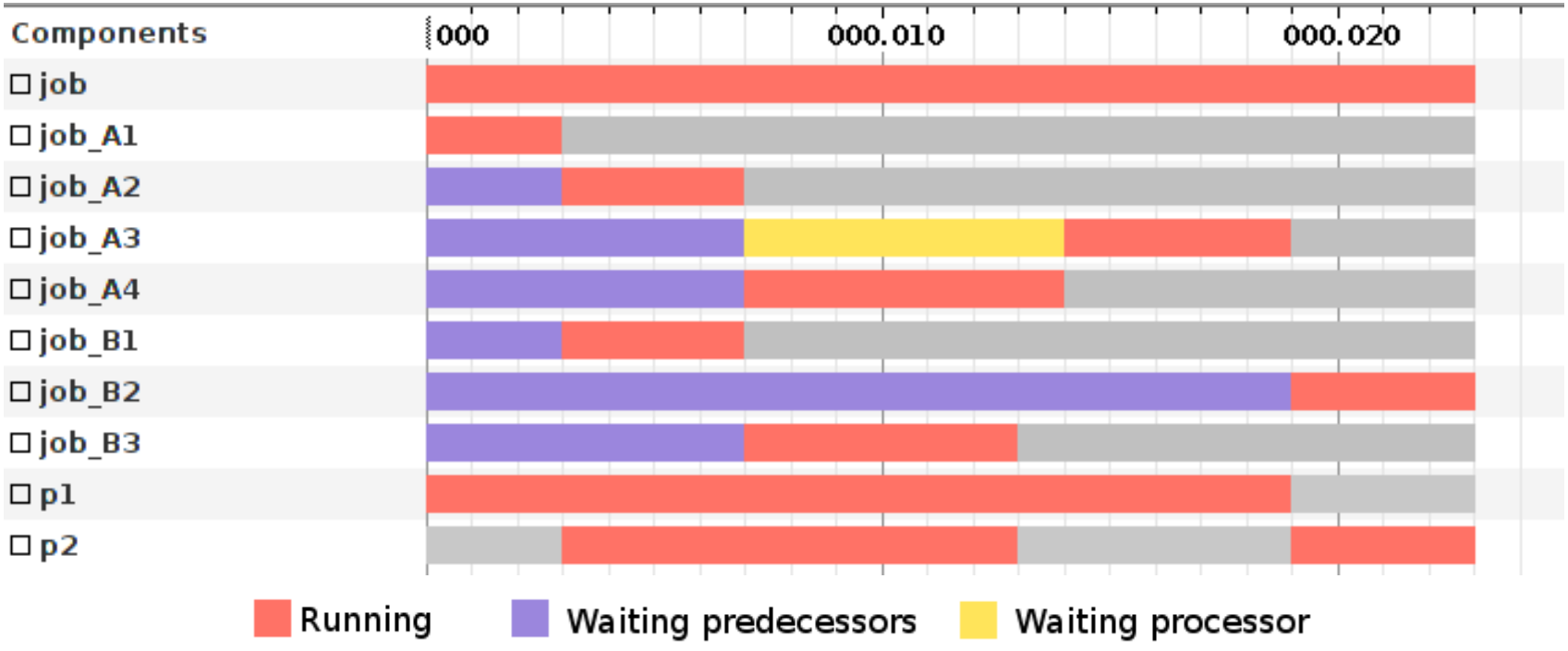
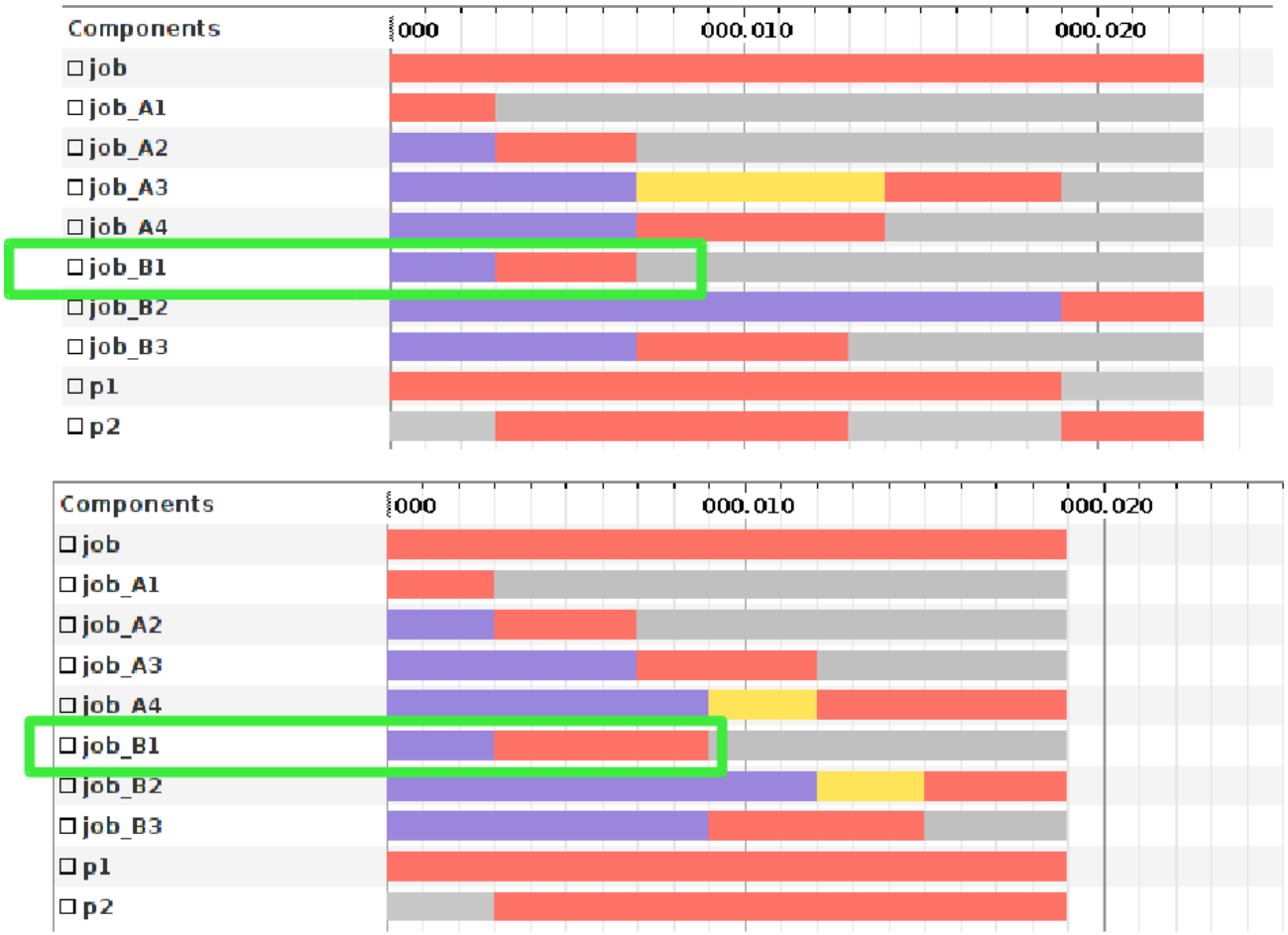


- Analysis gives a response time of 23 timeunits

Explanations



B1 takes less time $\Rightarrow$ A4 start before A3 (on critical path).

Quantitative Estimation

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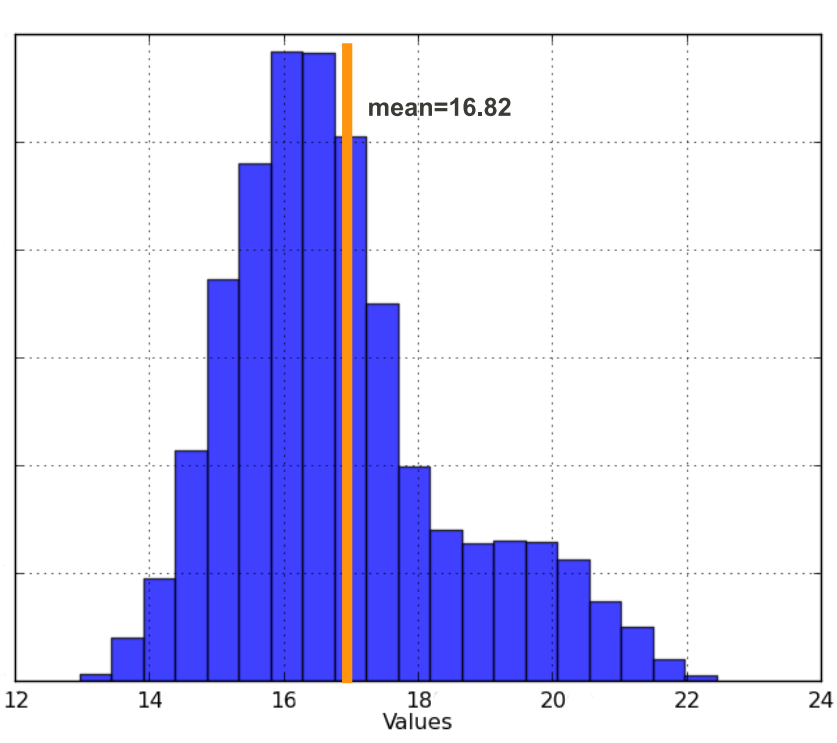
With simulation we get more quantitative information:



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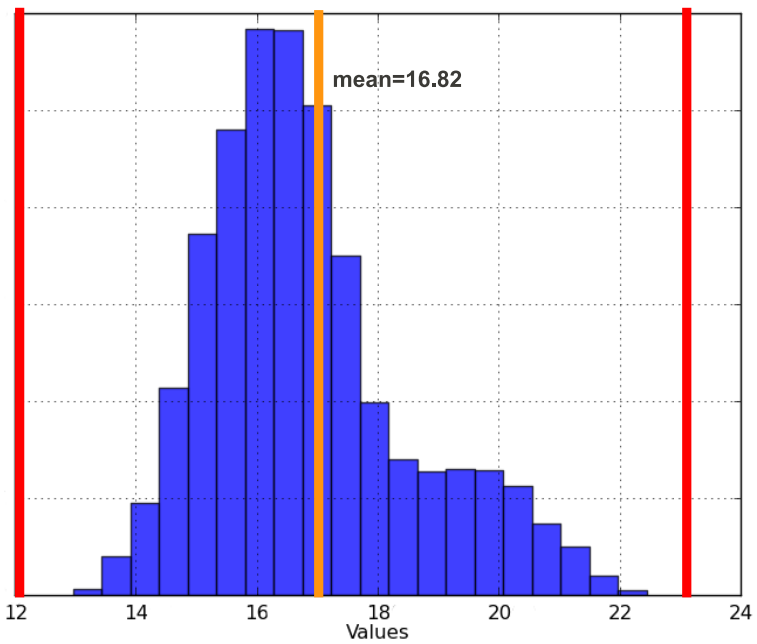
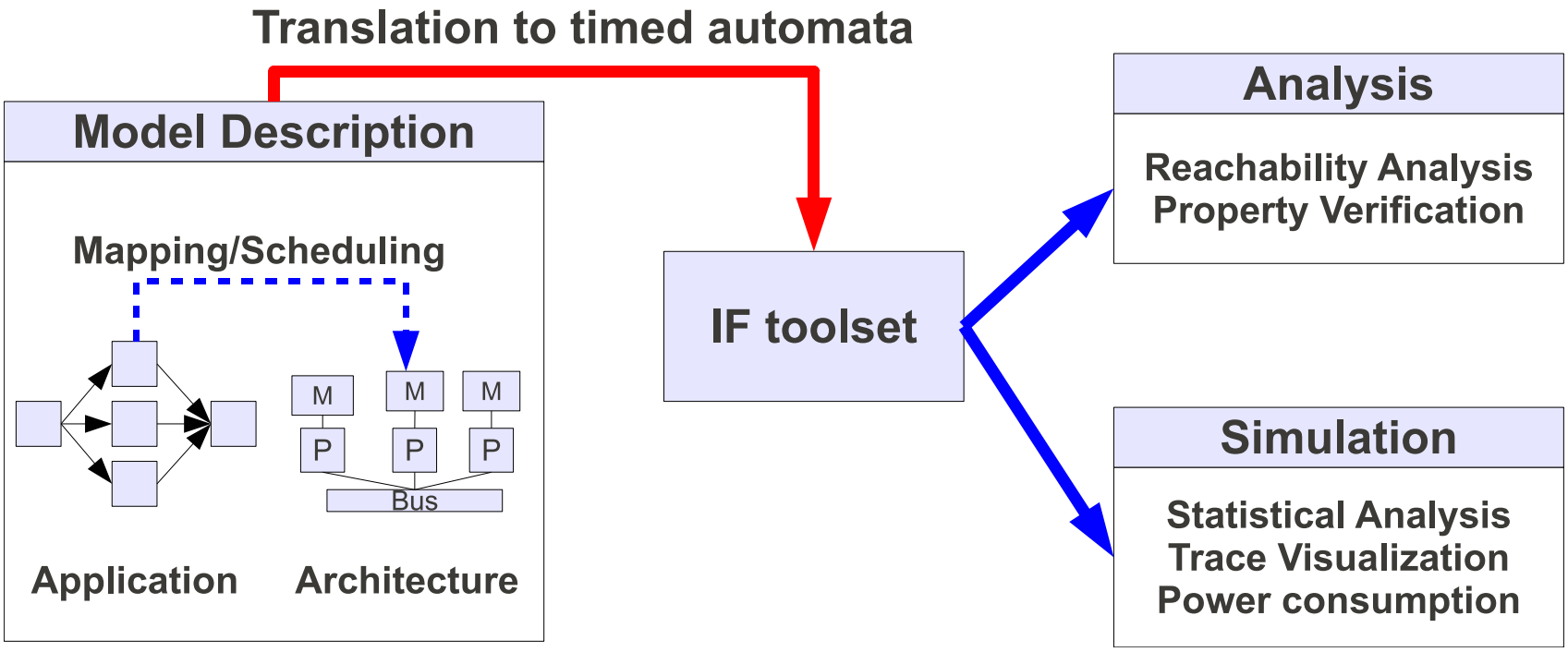


DeSpEx

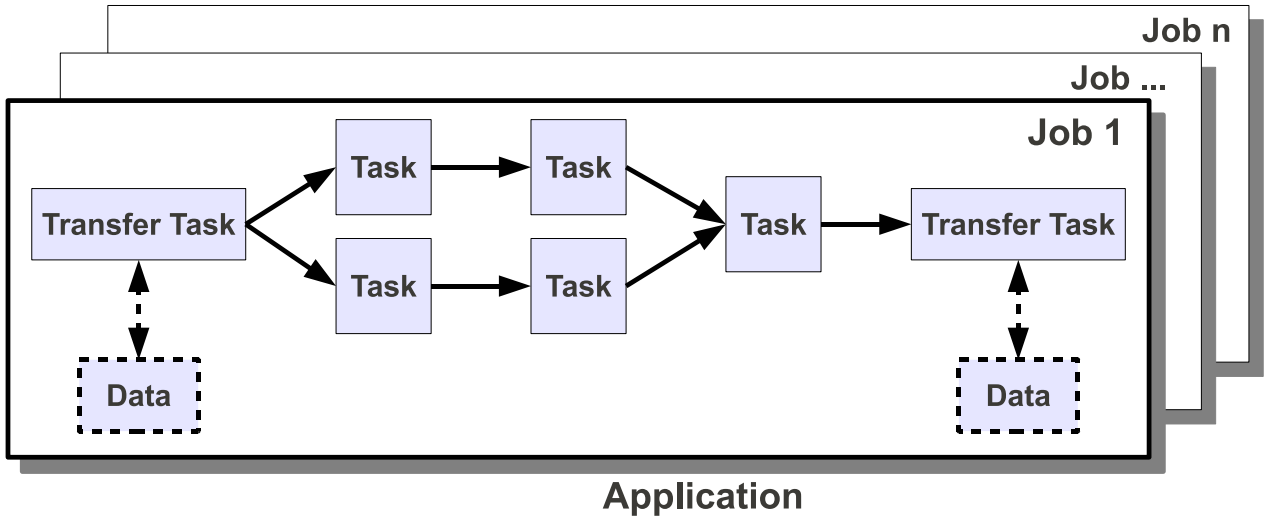
A framework for high level modeling and analysis

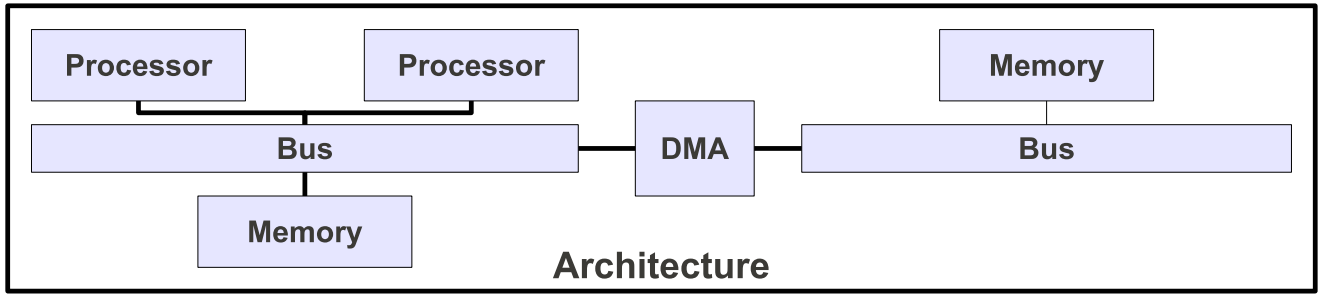
- Provide HW/SW designers with a framework for rapid design space exploration
- High level language for model description
- Formal semantics provided by *timed automata*
- Performance evaluation using formal methods and stochastic simulation

Framework Overview



Model overview





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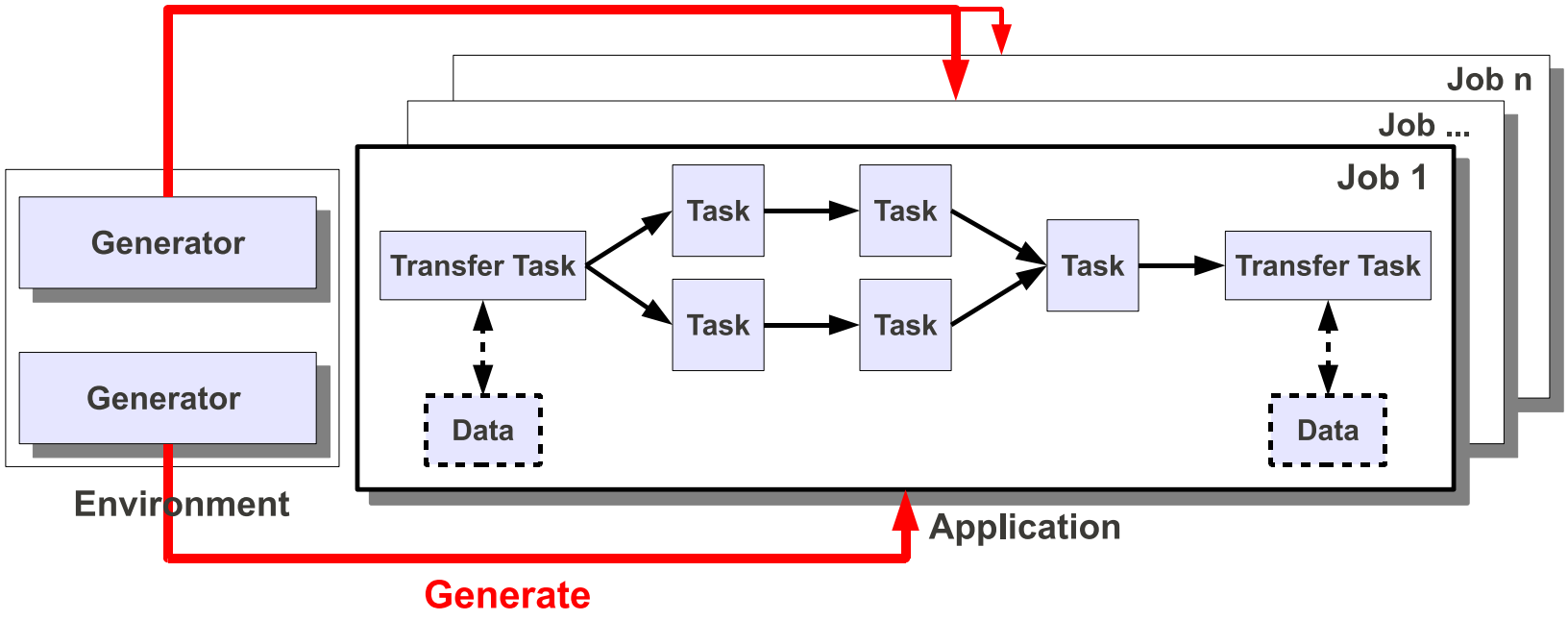

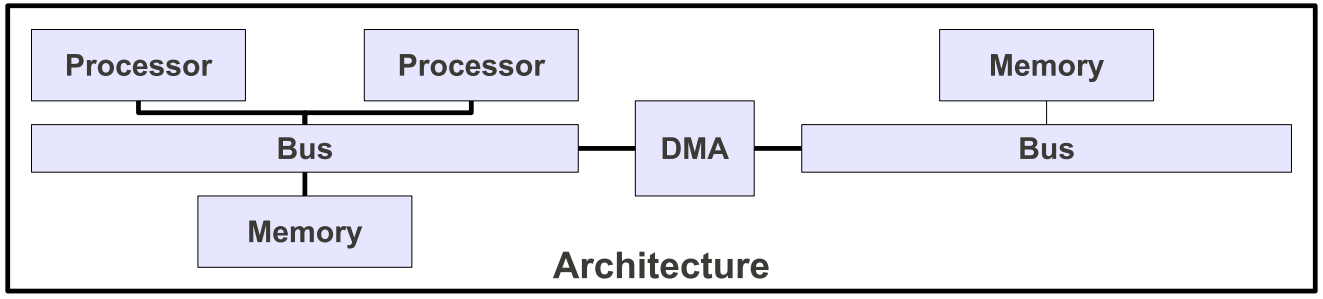

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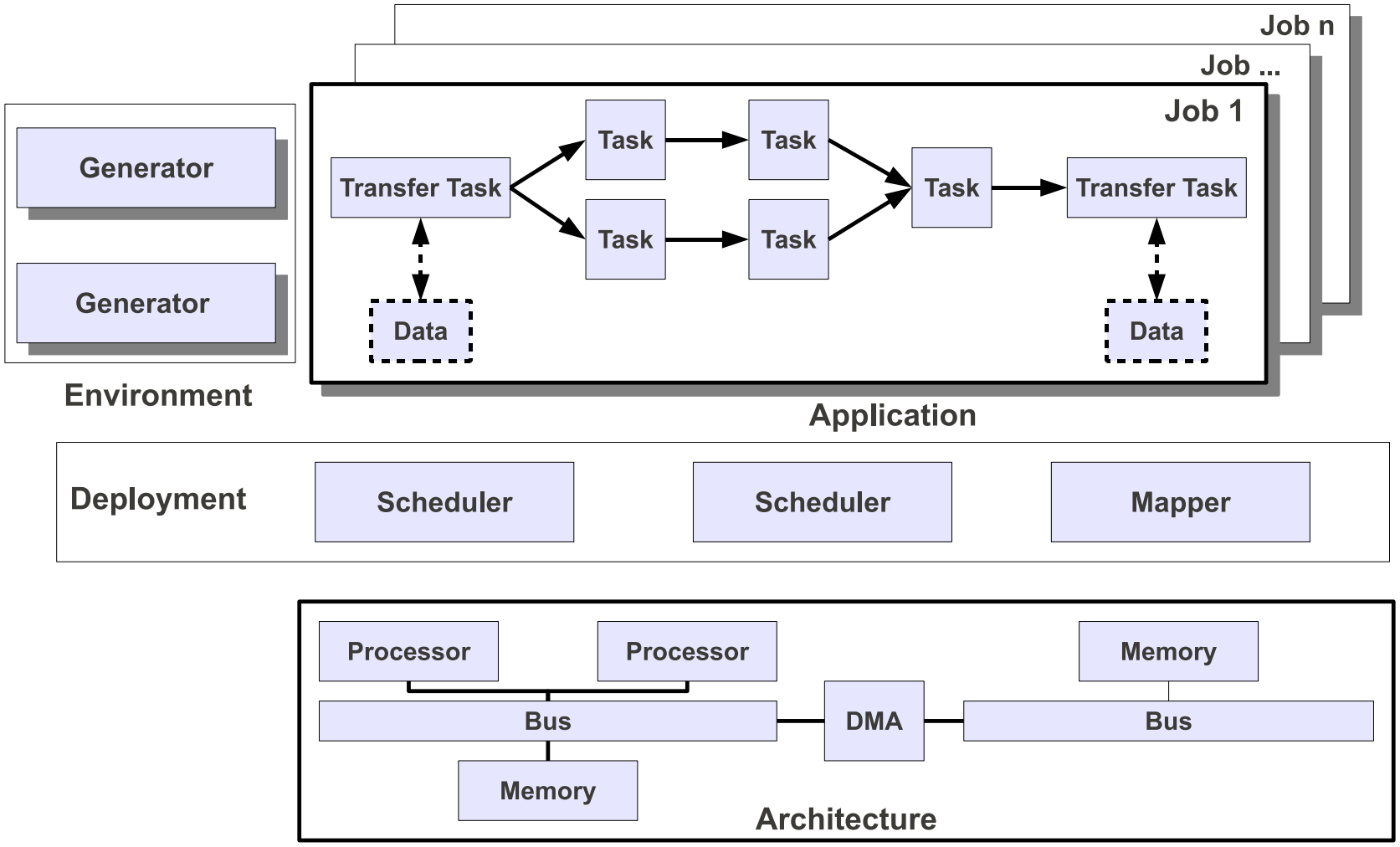

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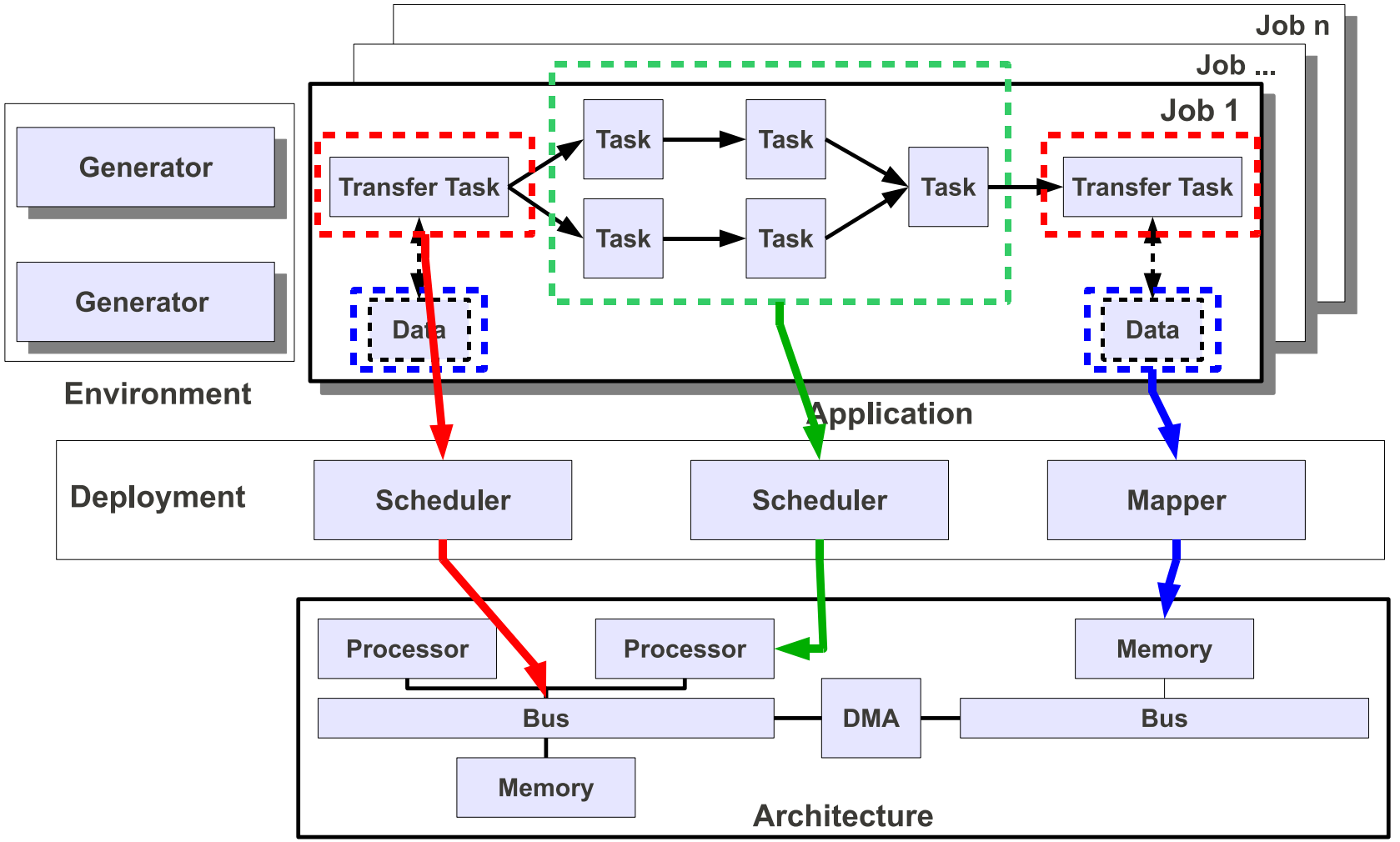

Evaluation

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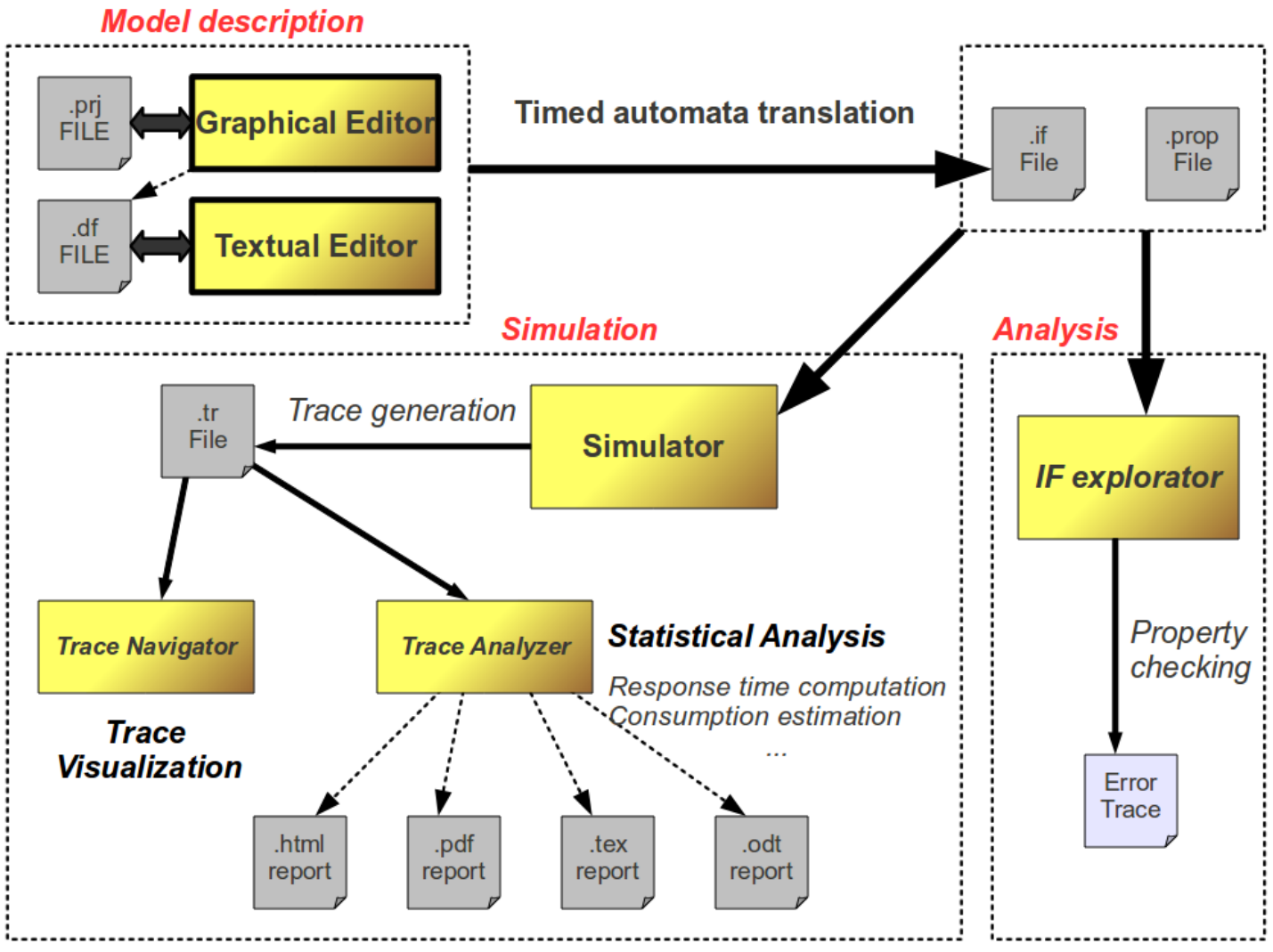
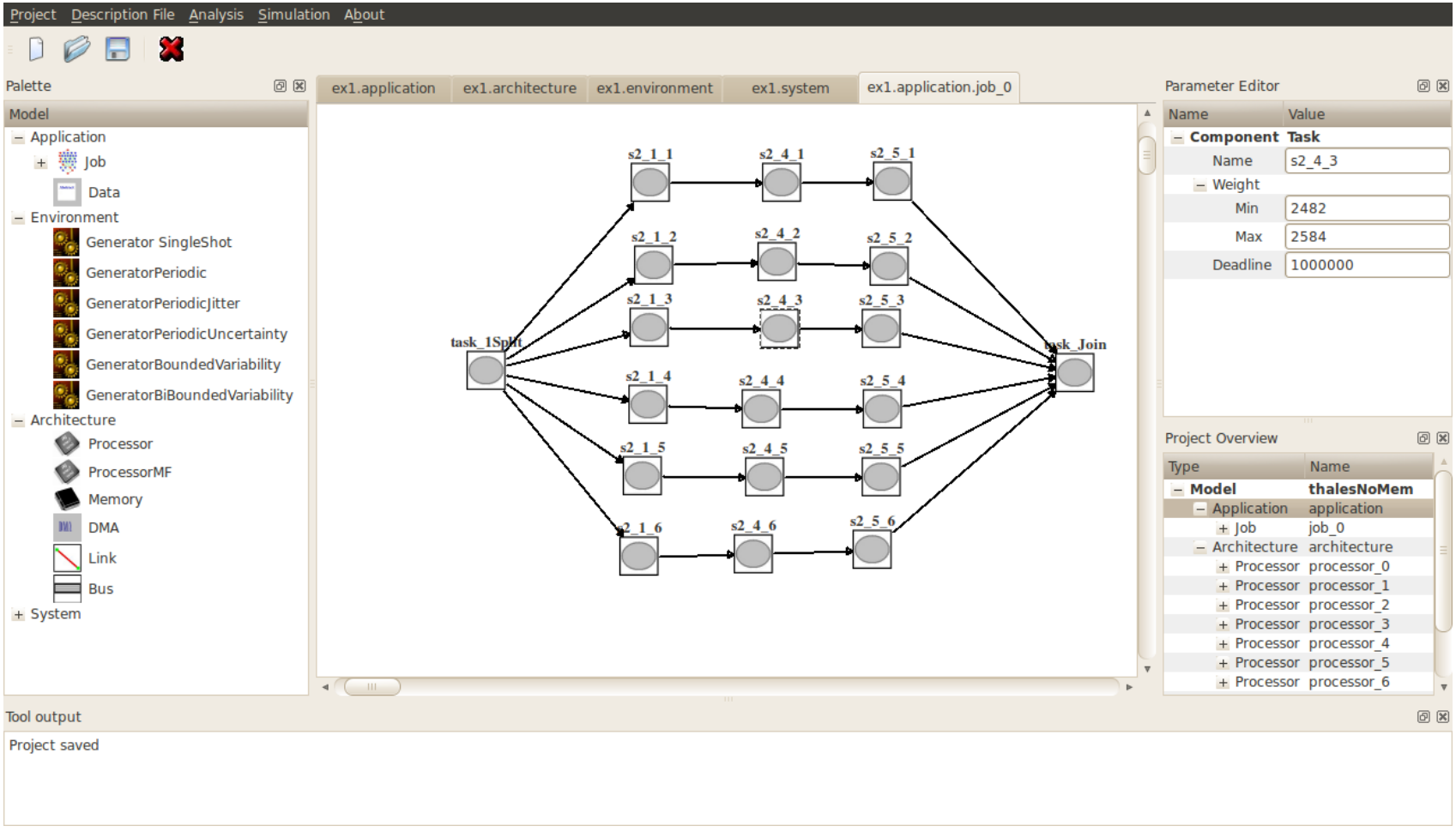
- For each component we generate a corresponding timed automaton model
- The composition of all automata yields a global timed automaton which captures the semantics of the system
- All our analysis methods are based on a **unified semantic model** provided by timed automata

Tool Overview

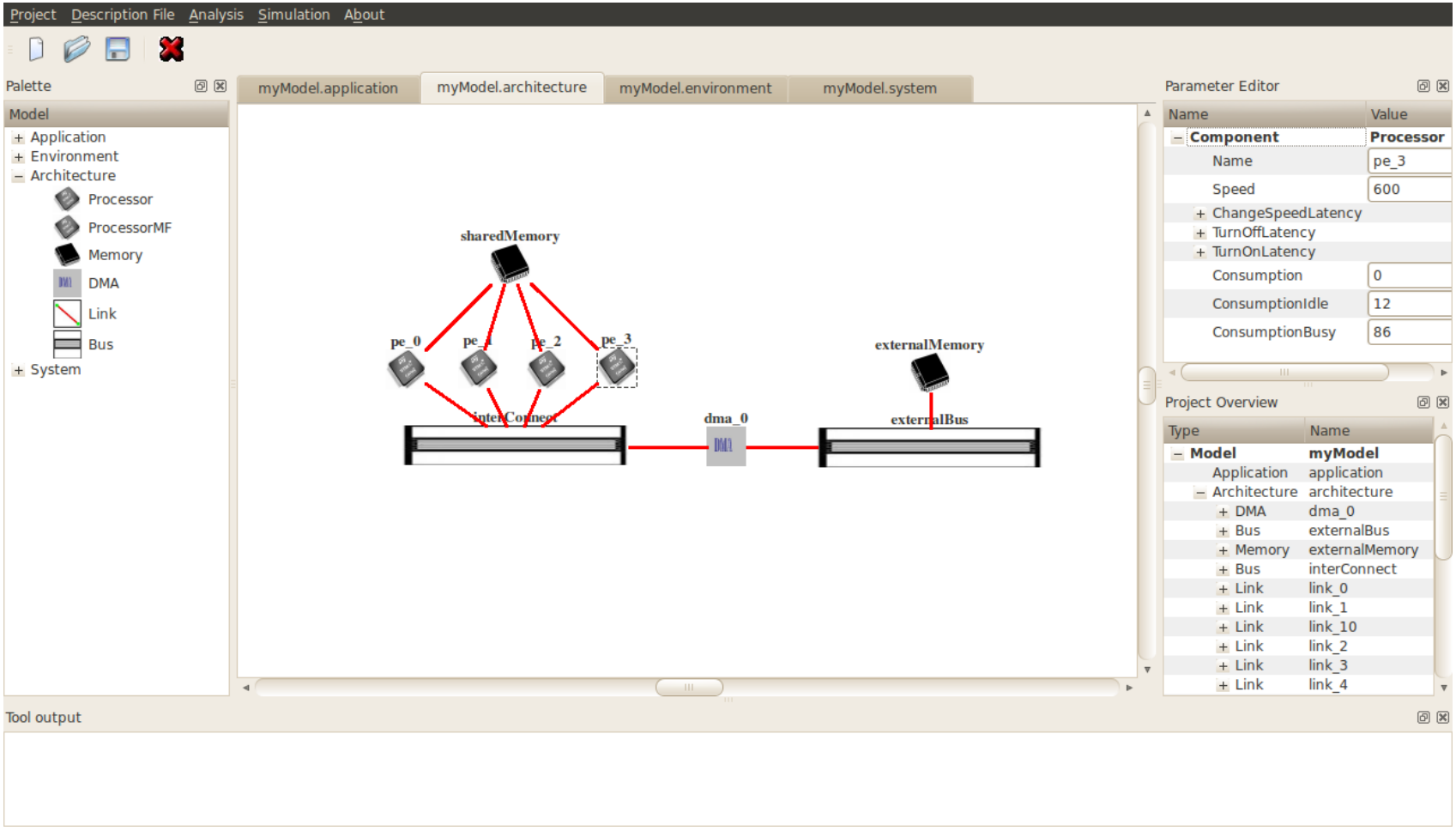


DeSpEx: Graphical Model Editor



DeSpEx: Graphical Model Editor

Architecture inspired by P2012 platform



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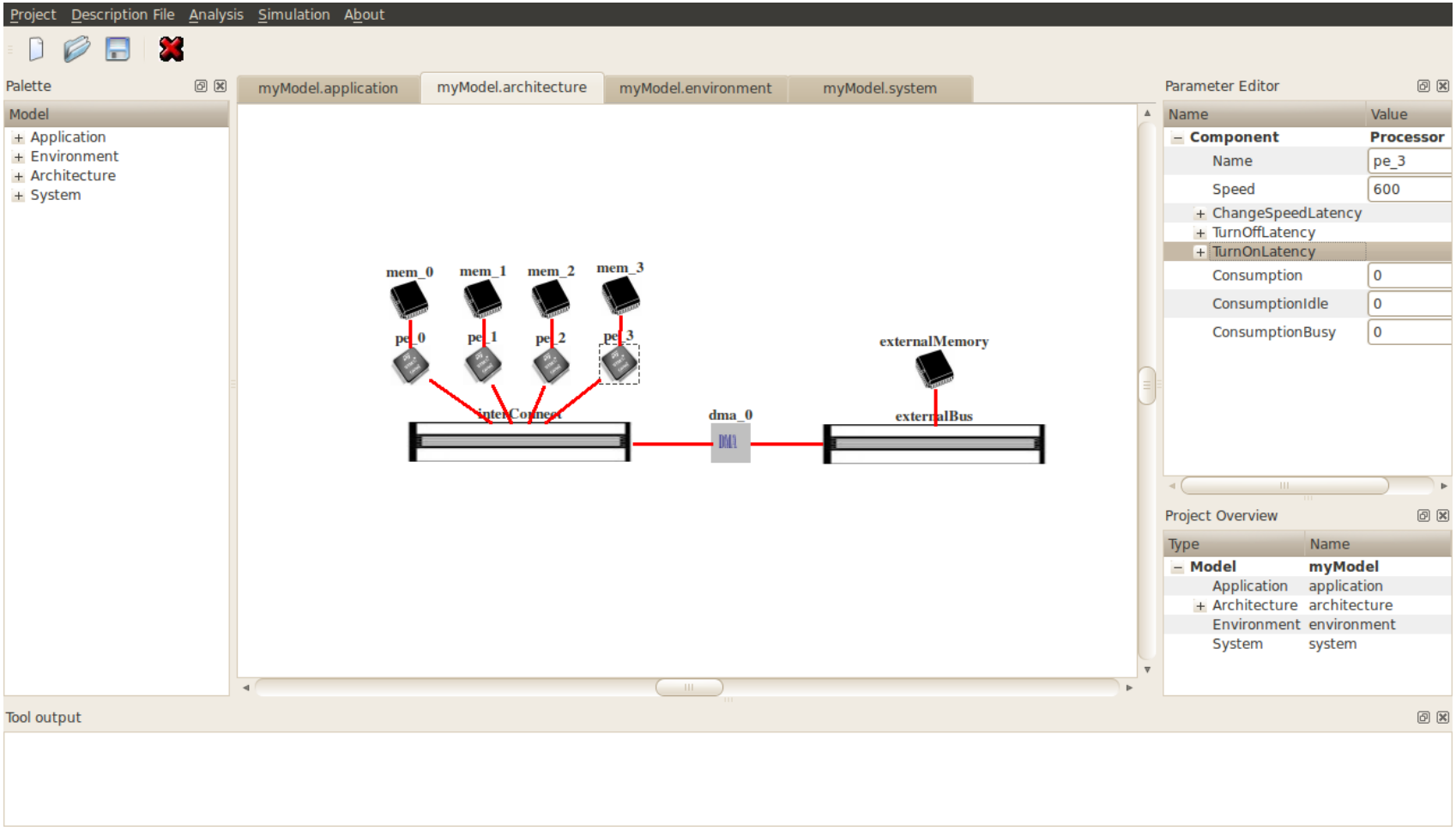
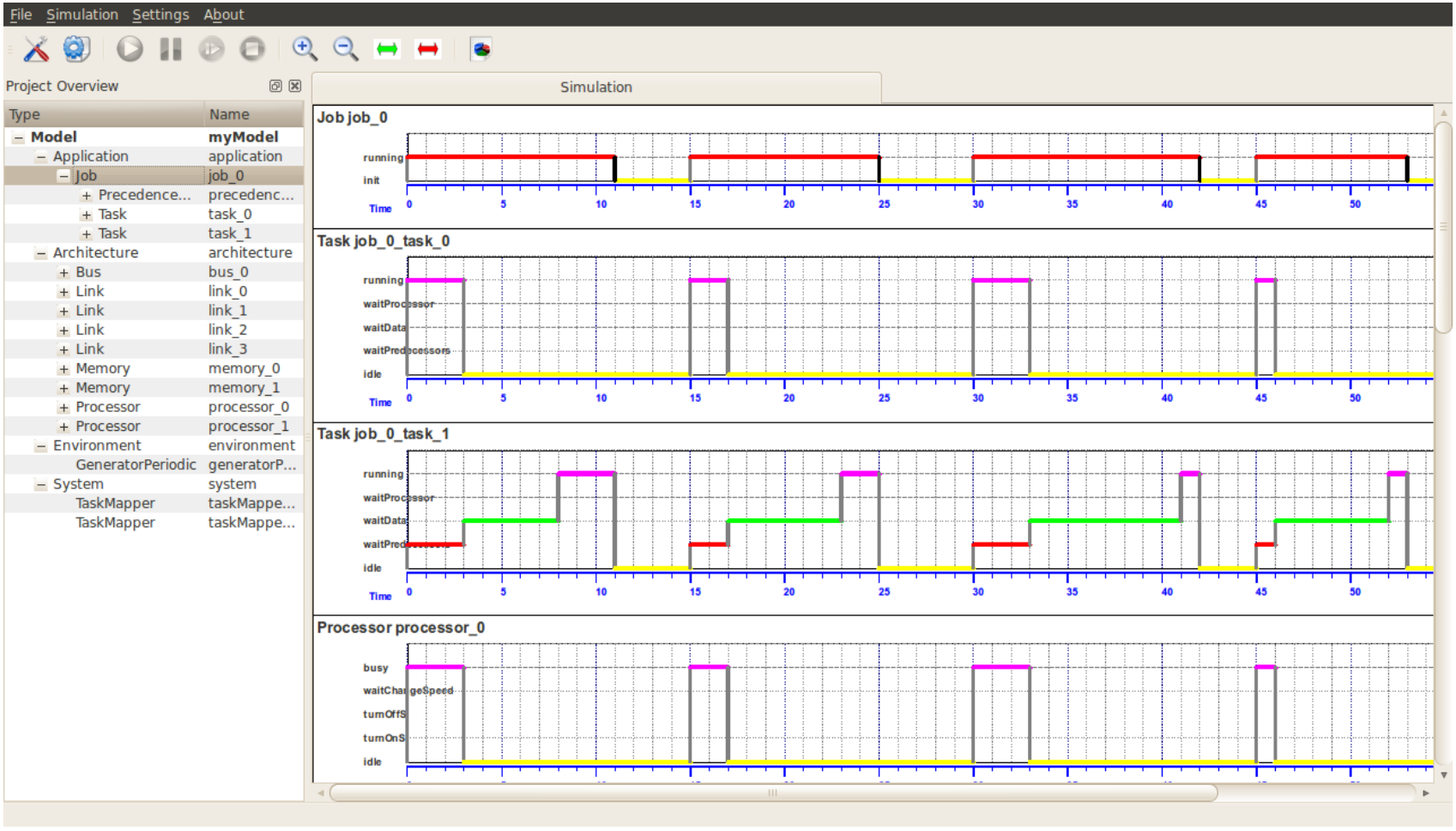
Architecture inspired by Cell platform



DeSpEx: Simulation and Trace Visualization



DeSpEx: Trace Visualization (Gantt Chart)

Performance Evaluation

Reachability Analysis

- Check whether some properties are satisfied or not
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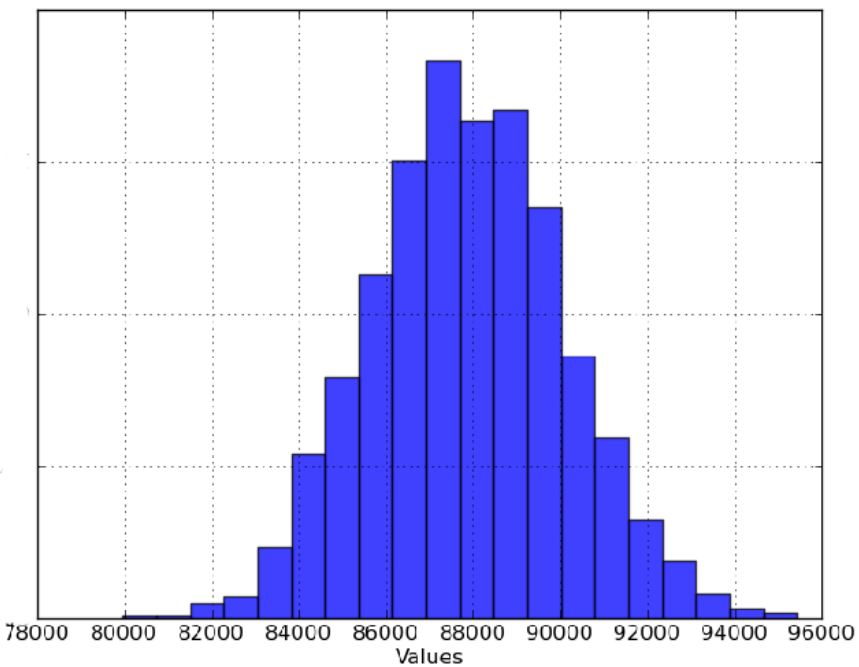
Stochastic Simulation

- Depending on the size of the model it may be difficult (sometimes impossible) to perform reachability analysis
- Timed automata are used to perform discrete event simulation:
  - **Semantic model is the same** as for reachability analysis
  - Randomized reachability exploration
  - We restrict ourself to bounded uncertainty

Performance Evaluation

Trace Analysis

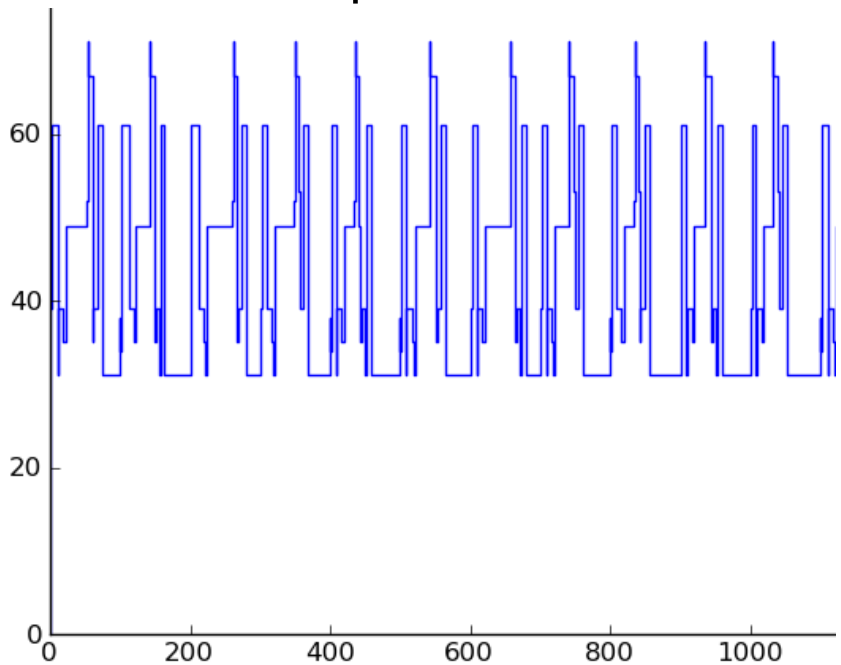
- Stochastic simulation generates timed traces
- We can retrieve quantitative informations with trace analysis:
  - Response time distribution of job



Performance Evaluation

Trace Analysis

- Stochastic simulation generates timed traces
- We can retrieve quantitative informations with trace analysis:
  - Response time distribution of job
  - Power consumption estimation



Case Study

Video Processing on P2012

Goal

- Demonstrate how DeSpEx can be used to solve realistic problems in design space exploration

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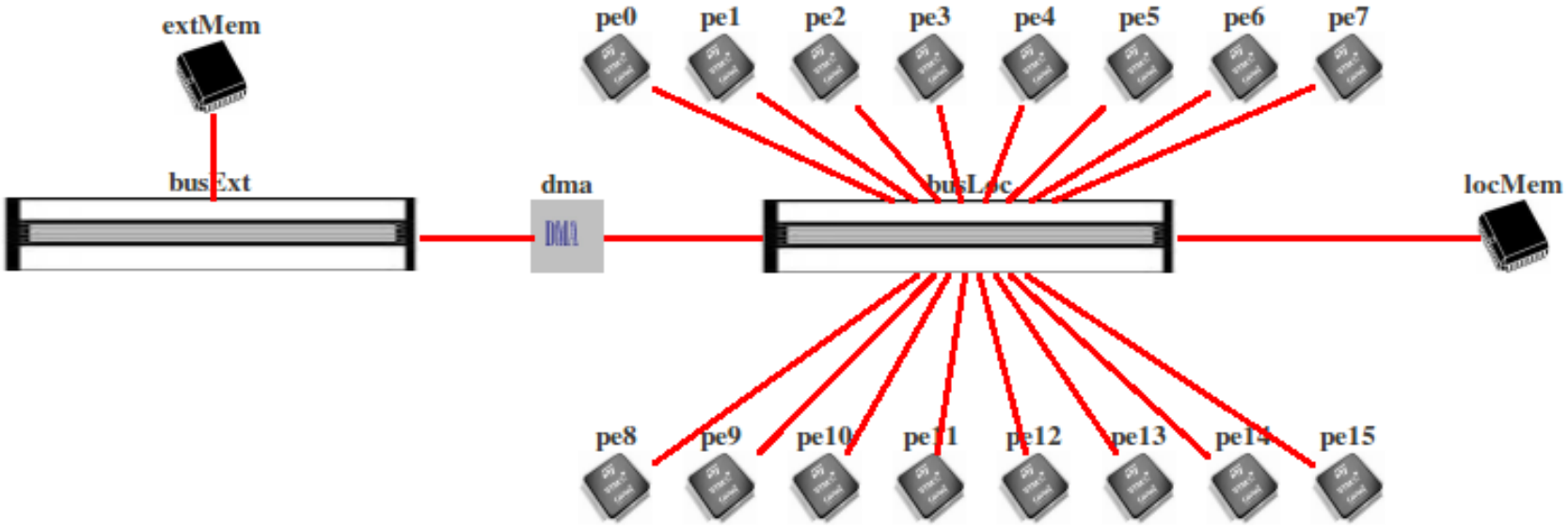
- Demonstrate how DeSpEx can be used to solve realistic problems in design space exploration
- Quantify the performance differences between different design choices
- Represent available cost/performance trade-offs.

Video Processing on P2012

Architecture Abstraction

- P2012 is a many-core computing fabric based on multiple clusters
- We restrict our models to one cluster

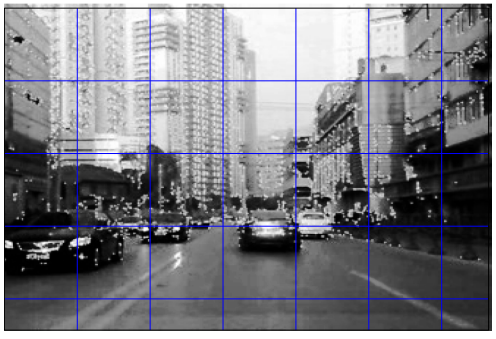


Video Processing on P2012

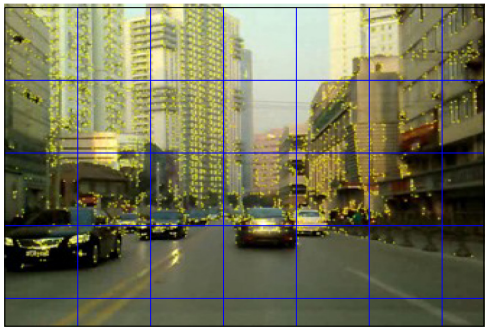
Application

- Augmented reality application called FAST
  (Features from Accelerated Segment Test)
- Corner detection method
- Algorithm consists in computing the detection on a chunk of an image

A



B



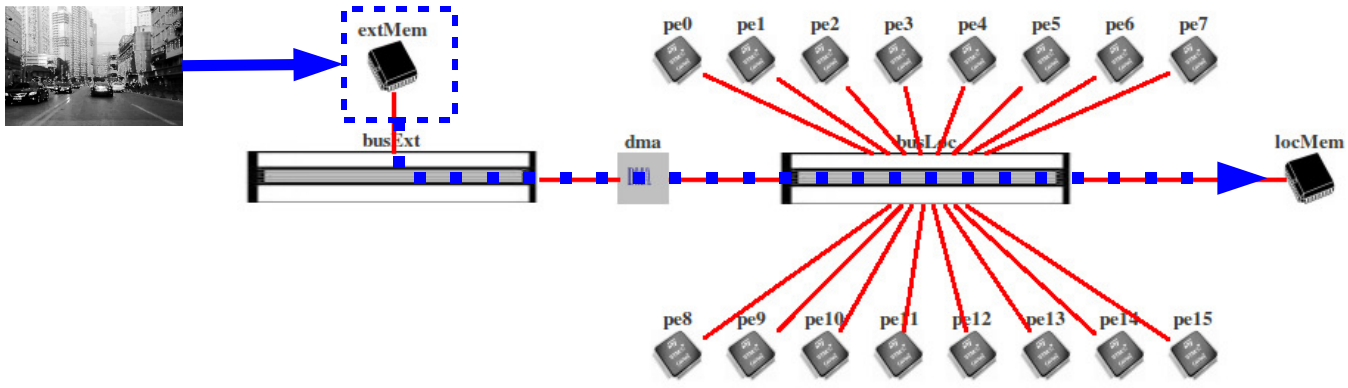
Algorithm

```
ForEach A[i][j]
Do
      B[i][j]:= compute(A[i][j])
EndDo
```

Video Processing on P2012

From an architectural point of view:

- The image resides initially in the off-chip memory
- Needs to be brought to local memory
- Then dispatched to processors for execution



Constraints:

- The whole image does not fit into the local memory
- Several alternatives for its splitting and transfer to local memories

Video Processing on P2012

At early design stage:

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Compare different design alternatives with DeSpEx

- How many processors should we use ? 1,2,4,8 or 16
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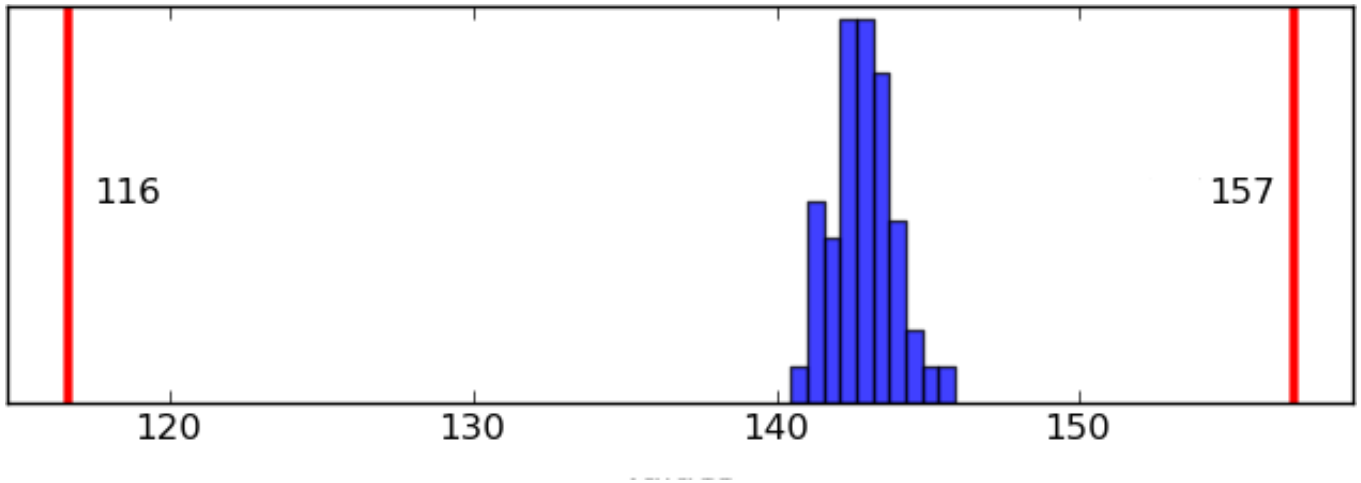
- Power consumption of the platform

Video Processing on P2012: Evaluation

Worst-Case vs Statistics

- Compare results from simulation and reachability analysis:



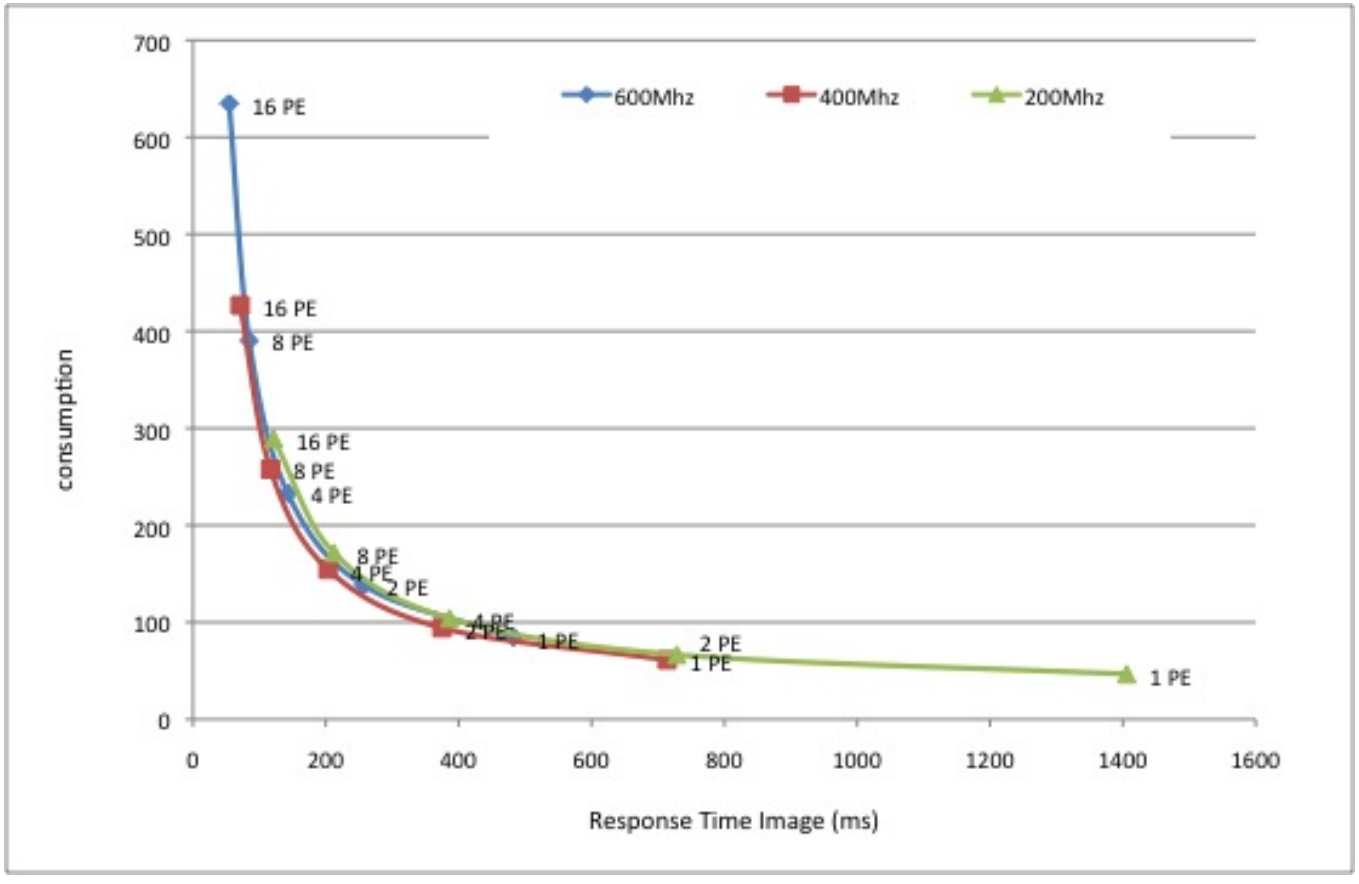
Response time of processing one image.

- Bands treatment
- 4 processors (600 MHz)

Video Processing on P2012: Evaluation

Power Consumption

We compare different configuration of the platform to get the trade-offs between response time and power consumption.



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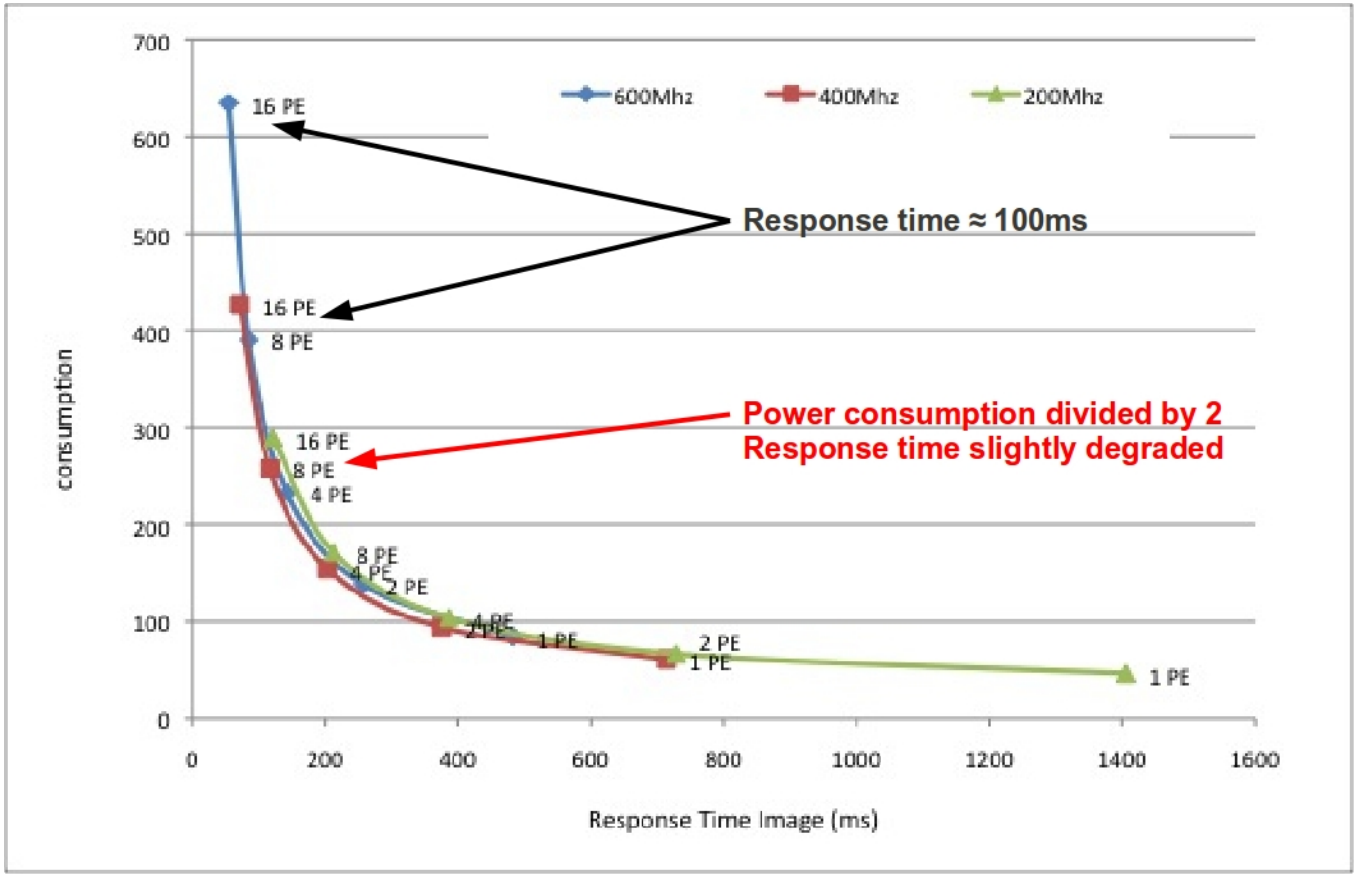

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Thank you for your attention

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