

February 2018

Oded Maler

Verimag

Centre Equation, 2, av. de Vignate

38610 Gières, France

E-Mail: maler@imag.fr

Phone: +33 (0) 456 52 03 74 Fax: 456 52 03 44

Personal Information:

- **Born:** 21 February 1957, Haifa, ISRAEL.
- **Situation:** Married, 2 children.
- **Nationality:** French and Israeli.
- **Personal address:** 7 chemin de Vence, 38700 Corenc, France; Tel: +33 (0)4 76-88-07-11

Research Interests:

- Verification, simulation, monitoring and synthesis for continuous and hybrid systems and their application (control, analog circuits, biology).
- Interaction between the mathematics of computation and traditional mathematics.
- Systems Biology.
- Theory and applications of automata and timed automata (timing analysis of software and hardware, planning and scheduling).
- Multi-criteria optimization, Machine learning, Multi-core computing.

Academic Degrees

- 1976 – 1979: B.A. in Computer Science, Department of Computer Science, Technion – Israel Institute of Technology, Haifa, Israel.
- 1980 – 1984 M.Sc. in Management Science – Information Systems, Recanatti School of Business Administration, Tel-Aviv University, Tel-Aviv, Israel. Thesis title: *Evidence Propagation and Control Strategies in Bayesian Inference Networks*. Supervisor: Moshe Ben-Bassat. (In parallel with 5-year military service).
- 1986 – 1990 Ph.D. in Computer Science, Department of Applied Mathematics and Computer Science, Weizmann Institute of Science, Rehovot, Israel. Thesis title: : *Finite Automata: Infinite Behavior, Learnability and Decomposition*. Supervisor: Amir Pnueli.
- 2000 – 2000 “Habilitation à diriger des recherches”: *Discrete, Timed and Hybrid Systems*, Univ. J. Fourier, Grenoble.

Academic Appointments

- 1990 – 1992: An associate researcher at IRISA, Rennes, France.
- 1992 – 1994: An associate researcher at VERIMAG, Grenoble, France.

- 1994 – 2001: A researcher (CR1) at the CNRS, VERIMAG, Grenoble, France.
- 2001 – 2011: A research director (DR2) at the CNRS, VERIMAG, Grenoble, France.
- 2011 – present: A research director (DR1) at the CNRS, VERIMAG, Grenoble, France.

Other Professional Experience:

- 1977 – 1979: Vice-editor and editor of *Epsilon* – the Technion students magazine.
- 1979 – 1984: Programmer, software designer, data-base administrator and system analyst in the Israeli army.
- 1984 – 1986: Research employee in the Weizmann Institute in areas related to the application of Logic Programming in education. Teaching in a high-school. Consultation services for an electronics company in building expert systems. Writing in the Israeli *Computer and People* magazine and in *Ha-aretz* daily newspaper.
- 2002 – 2003: Consultant for Astrium SA on automatic generation of embedded software from high level specifications.
- 2012 – 2015: Member of the technical advisory board of ATRENTA Inc.

Long-term visits

- University of California, Berkeley, summers of 1997-2000.
- Carnegie-Mellon University, Pittsburgh, summers of 2001-05.
- University of Pennsylvania, Philadelphia, summer 2006.
- Weizmann Institute, Rehovot, winter 2009 (3 months).
- Stony Brook University, New York, summer 2011.
- Embedded Systems Institute, Eindhoven, summer 2012.
- Toyota Research Center, Los Angeles, summers 2014-16

Administrative Responsibilities

- Head of the *timed and hybrid group* (TEMPO) at VERIMAG (10-15 persons) since 1999.
- Member of the laboratory council of VERIMAG
- Member of the bureau of VERIMAG

Teaching Experience

- 1983: Teaching an introductory programming course at the faculty of management, Tel-Aviv University.
- 1984 – 1986: Preparing a curriculum for teaching Logic and Logic Programming for high school. Teaching this subject at a school in Ramat-Hasharon (Israel).

- 1984 – 1986: Conducting Prolog courses in various industrial and software companies (Israel).
- 1991: Teaching a master's (DESS) course on advanced topics in automata theory, IFSIC, Rennes.
- 1997-1998: Teaching an advanced under-graduate (magistère) course on verification using automata and timed automata, Univ. J. Fourier, Grenoble.
- 1999: Mini-course on hybrid systems in Marseille.
- 2000: Mini-course on hybrid systems in Murcia, Spain.
- 2001: Advanced course on timed and hybrid systems, Univ. J. Fourier, Grenoble.
- 2003: Advanced course on timed and hybrid systems, Univ. J. Fourier, Grenoble.
- 2003: A tutorial on timed automata for planning and scheduling, ICAPS'93, Trento.
- 2005: Advanced course on timed and hybrid systems, Univ. J. Fourier, Grenoble.
- 2007: Advanced course on timed and hybrid systems, Univ. J. Fourier, Grenoble.
- 2012: Lecturing in a spring school of the French Society for Theoretical Biology, St Flour.
- 2012: Program committee of the MOVEP winter school, Marseille.
- 2013: Lecturing in the International school on formal methods, Bertinoro, Italy.
- 2013: Advanced course on cyber-physical systems, Technical university of Vienna.
- 2013: Lecturing in Nano-Terra summer school, Aix-les-Bains.
- 2017: Advanced course on research topics in timed and hybrid systems, University of Grenoble-Alpes.

Organization of Workshops and Schools:

- European workshop on hybrid systems, Grenoble, 1995 (organizer and PC chair).
- Workshop on hybrid and real-time systems, Grenoble 1997 (organizer and PC chair).
- Autumn school “computational aspects and applications of hybrid systems”, Grenoble, 1998.
- Spring school “modelisation, test et validation”, Marseille, 1999.
- Workshop on theory and practice of timed systems, Grenoble, 2002 (organizer and PC chair).
- Member of the steering committee of *HSCC, Hybrid Systems: Computation and Control*, since 1998 (chair 2003-2006).
- Chair of the steering committee of *FORMATS: Formal Methods for Real-time Systems*, since 2003.
- Organizer and PC chair of *FAC: workshop on Formal Verification of Analog Circuits*, Edinburgh, 2005.

- Organizer of the international workshop *Topics in Computation and control*, Santa Barbara, 2006.
- Organizer of the international workshop *Between Control and Software*, Grenoble, 2007.
- Organizer of the international workshop *Toward Systems Biology*, Grenoble, 2007.
- Organizer and PC co-chair of *FAC: 2nd workshop on Formal Verification of Analog Circuits*, Princeton, 2008.
- PC co-chair of *CAV: 21st conference on Computer-Aided Verification*, Grenoble 2009.
- Organizer of the second international workshop *Toward Systems Biology*, Grenoble, 2011.
- Member of the steering committee of *FAC: Frontiers in Analog CAD* since 2010.
- Member of the steering committee of *Hybrid Systems Biology* since 2013.
- Organization of a workshop *Formal and Informal Methods for Verification and Performance*, Marrakesh, Morocco, 2013.
- PC co-chair of the 3rd workshop *Hybrid Systems Biology*, Vienna, 2014.
- PC co-chair, *1st Workshop on Monitoring and Testing of Cyber-Physical Systems*, Vienna, 2016.
- General chair of the 5th workshop *Hybrid Systems Biology*, Grenoble, 2016.

Membership in Program Committees and Editorial Boards:

- *Hybrid Systems III* (Rutgers, 1995), IV (Cornell, 1996), V (Notre-Dame, 1997).
- *Hybrid Systems: Computation and Control (HSCC)*, 1998 (Berkeley), 1999 (Nijmegen), 2000 (Pittsburgh), 2001 (Rome), 2002, (Palo Alto), 2003 (Prague, co-chair).
- *Int. Conference on Concurrency Theory (CONCUR)*, 1998 (Nice), 2001 (Aalborg).
- *Workshop on Application of Concurrency in System Design (ACSD)*, 2001 (Newcastle), 2004 (Hamilton).
- *Foundation of Software Technology and Theoretical Computer Science (FST/TCS)*, 2001 (Bangalore), 2008 (Kanpur), 2012 (Hyderabad).
- *European Journal of Control* (1999-2006).
- *Logic in Computer Science (LICS)*, 2002 (Copenhagen).
- *Formal Methods in Real-Time and Fault-Tolerant Computing (FTRTFT)*, 2002 (Oldenburg).
- *Formal Methods for Timed systems (FORMATS)*, 2003 (Marseille), 2005 (Uppsala), 2009 (Budapest), 2015 (Madrid), 2016 (Quebec City).
- *Computer-Aided Verification (CAV)*, 2004 (Boston), 2008 (Princeton), 2009 (Grenoble, PC co-chair), 2010 (Edinburgh).
- *Formal Methods in Computer-Aided Design (FMCAD)*, 2010 (Lugano), 2011 (Austin).

- *Computational Methods in Systems Biology (CMSB)*, 2011 (Bologna), 2013 (Vienna), 2016 (Cambridge, UK), 2017 (Darmstadt)
- *Hybrid Systems Biology (HSB)*, 2012 (Taormina), 2013 (Vienna), 2015 (Madrid), 2016 (Grenoble).
- *Euromicoro Conference on Real-Time Systems (ECRTS)*, 2011 (Porto).
- *Runtime Verification (RV)*, 2012 (Istanbul), 2013 (Rennes), 2015 (Vienna), 2016 (Madrid).
- *Haife Verification Conference*, 2013.
- *Automata, Languages and Programming (ICALP)*, 2014 (Copenhagen).
- *Principles of Distributed Computing (PODC)*, 2014 (Paris).
- *Automated Technology for Verification and Analysis (ATVA)*, 2014 (Sydney).
- *Monitoring Cyber-Physical Systems (MT-CPS)*, 2016 (Vienna), 2017 (Pittsburgh).
- *Analysis and Design of Hybrid Systems (ADHS)*, 2003 (St Malo), 2015 (Atlanta).
- *International Conference on Language and Automata Theory and Applications (LATA)*, 2016 (Prague).

Invited Presentations

1. *Workshop on Reactive Systems and Model Checking: from Concept to Tool*, Uppsala, Sweden, 1998.
2. *2nd Int. Workshop on Probabilistic Methods in Verification*, Eindhoven, Netherlands, 1999.
3. *Workshop on Reactive Systems*, Oldenburg, 2000.
4. *2nd IFAC Symposium on Nonlinear Control Systems (NOLCOS 2001)*, Saint-Petersburg, Russia, 2001
5. *7th IFAC Workshop on Discrete Event Systems (WODES 2004)*, Reims, France, 2004.
6. *Joint Colloquium Distinguished Lecture Series*, UC Berkeley, Berkeley, USA, 2005.
7. *6th International Workshop on Automated Verification of Critical Systems (AVOCS)*, Nancy, France, 2006.
8. *1st Workshop on Omega-Automata*, Tokyo, Japan, 2007.
9. *Workshop on Formal Methods in Systems Biology*, Cambridge UK, 2008.
10. *McKay Lectures*, UC Berkeley, 2008.
11. *Workshop on the Reachability Problem*, Paris, 2009.
12. *Cyber-Physical Week*, Stockholm, 2010.
13. *Amir Pnueli Memorial Symposium*, New York, 2010.

14. *4th Workshop on Theorem Proving*, Belgrade, 2011.
15. *Workshop on Formal Methods in Robotics*, Salt-Lake City, 2011.
16. *FORMATS: Formal Methods for Real-time Systems*, Aalborg, 2011.
17. *EMSOFT: Embedded Software*, Taipei, 2011.
18. *Infinity workshop*, Hanoi, 2013.
19. *QAPL workshop*, Grenoble, 2014.
20. *Workshop: Dynamic Biological Modeling: Abstractions, Algorithms and Logic*, Berkeley, 2015.
21. *Meeting of the BIOSS working group on Computational Biology*, Paris, 2015.
22. *Int. conference on Runtime Verification (RV)*, Madrid, 2016.

Research Supervision

- Since 1999: Leader of the “Timed and Hybrid Systems” group at VERIMAG.
- Post-docs
 - 1998 – 2000: Peter Niebert, Modeling, Verification and Optimization of Industrial Plants using Timed and Hybrid Models
 - 1999 – 2000: Hou Jianmin, Timing Analysis of Asynchronous Circuits
 - 2005 – 2006: Goren Frehse, Verification of Hybrid Systems.
 - 2005 – 2006: Antoine Girard, Efficient Reachability Computation
 - 2006 – 2007: Gregory Batt, Hybrid Techniques for Biology
 - 2007 – 2008: Victor Schuppan, Controller Synthesis
 - 2007 – 2009: Ramzi Ben Salah, Compositional Timing Analysis
 - 2008 – 2011: Alexandre Donze, Parameter Synthesis for Biological Models
 - 2009 – 2010: Scott Cotton, Optimization and Satisfaction
 - 2010 – 2011: Jiansheng Xing, Multi-core Performance Evaluation.
 - 2013 – 2015: Stefano Minopoli, Monitoring and Reachability
 - 2016 – 2017: Marcelo Forets, Hybrid Systems for Electrical Applications
- Ph.D. Students – Supervision
 - 1996 – 2000: Thao Dang, INP Grenoble: *Verification and Synthesis of Hybrid Systems*.
 - 1998 – 2002: Yasmina Abdellaïm, INP Grenoble: *Scheduling using Timed Automata*.
 - 2000 – 2003: Moez Mahfoudh, UJF Grenoble: *Timed Verification by Constraint Satisfaction*.
 - 2002 – 2006: Abdelkarin Kerbaa, UJF Grenoble: *Conditional Scheduling Strategies using Timed Automata*.
 - 2003 – 2007: Alexandre Donzé, UJF Grenoble: *Trajectory-based Techniques for Verification and Control*.

- 2003 – 2007: Ramzi Ben Salah, INP Grenoble: *Analysis of Large Timed Systems and Circuits*
 - 2004 – 2008: Dejan Nickovic, UJF Grenoble: *Checking Timed and Hybrid Properties*
 - 2005 – 2009, Scott Cotton, UJF Grenoble: *On Some Problems in Satisfiability Solving*
 - 2006 – 2009: Colas Le Guernic, UJF, Grenoble: *Reachability Analysis for Hybrid Systems*
 - 2006 – 2009, Aldric Degorre, UJF, Grenoble: *On some Quantitative Aspects of Formal Languages*
 - 2008 – 2011, Julien Legriel, UJF, Grenoble: *Multi-Criteria Optimization for Mapping and Scheduling on Multi Processors*
 - 2008 – 2012, Selma Saidi, UJF, Grenoble: *Optimizing DMA Data Transfers for Embedded Multi-Cores*
 - 2008 – 2012, Jean-Francois Kempf, UJF, Grenoble: *On Computer-Aided Design-Space Exploration for Multi-Cores*
 - 2010 – 2014, Pranav Tendulkar, UJF, Grenoble: *Efficient Deployment of Dataflow Programs on Multi-Core Computers*
 - 2012 – 2016, Jan Lanik, *CPower Reduction in Digital Circuits*
 - 2013 – 2016, Thomas Ferrere, *Assertion and Measurements for Mixed-Signal Simulation*
 - 2013 – 2017, Abhinav Srivastav, *On Theoretical and Practical Aspects of Trade-offs in Resource Allocation Problems*
 - 2012 – 2017, Irini-Eleftheria Mens, *Learning over Large Alphabets*
 - 2014 – 2018, Dogan Ulus, *Pattern Matching using Regular Expressions*
- Ph.D. Students – Partial Supervision
 - 1997 – 1998: Olivier Bournez, ENS Lyon: *Representation of Polyhedra*
 - 1996 – 2000: Marius Bozga, UJF Grenoble: *Efficient Verification of Timed and Probabilistic Systems*
 - 2001 – 2002: Catalin Dima, UJF Grenoble, *Algebraic Theory of Timed Automata*
 - 2004 – 2007: Tarik Nahhal, UJF Grenoble: *Test Generation for Continuous and Hybrid Systems*
 - 2008 – 2012: Rajarshi Ray, UJF Grenoble: *Tools for Hybrid Verification*
 - 2009 – 2012: Romain Testylier, UJF Grenoble: *Reachability for Nonlinear Systems*
- Masters Students
 - 2002 : Mathieu Moy, Timed Regular Expressions.
 - 2002 : Abdelkarim Kerbaa, Scheduling on Parallel Machines.
 - 2003 : Ramzi Ben Salah, Circuit Timing Analysis.
 - 2003 : Olfa Ben Sik Ali, Control Synthesis based on Search.
 - 2003 : Alexandre Donzè, Control and Observation of Piecewise-Affine Systems.
 - 2005 : Scott Cotton, SAT and Difference Constraints.
 - 2005 : Colas Le Guernic, Efficient Algorithms for Reachability Computation

- Interns (between 2 and 10 months)

Moez Mahfoudh, Manipulation of Timed Polyhedra (00), Ashwani Kumar, Modeling an Verification of Probabilistic Processes (00), Nishant Sharma, Efficient Probabilistic Verification (00), Sorav Bansal, Reachability Analysis of a Double Pendulum (00), Nishant Sinha, Verification of Domino Circuits with OpenKronos (00), Amri Amin, Verification of Non-Linear Hybrid Systems (01), Tarek El Mhamdi, Verification of Probabilistic Systems (01), Fadhel Graiet, Timed Verification of Circuits using Abstraction (01), Nishant Sharma, Efficient Algorithms for Non-Convex Polyhedra (01), Navendu Jain, Translation from Kronos to Difference Logic (01), Maud Salvoldi, Systematic Simulation of Continuous Systems (01), Bara Diop, Circuit Timing Analysis (02), Olfa Ben Sik Ali, Abstraction of Circuits (02), Ramzi Ben Salah, Verification of Large Circuits using Kronos (02), Dejan Nickovic, Monitoring Properties of Analog Signals (03), Sam Shapero, Search-based Recovery for Power Transmission Networks (03), Scott Cotton, Conflict Analysis in Hybrid SAT Solving (03), Ahmed Chaari, Instruction Scheduling using Timed Automata (05), Ramzi Marrouchi, Algorithms for Timed Synthesis (07), Mohamed Handous, Abstraction of Timed Systems (07), Gayathri Nair, Timed Modeling of Gene Networks (07), Parasara Sridhar, Analyzing Multi-Affine Functions (08), Rohith Reddy, Nonlinear Reachability (09), Manish Goayal, Verification by Simulation (09), Krishna Kanhaiya, Finding Zeros of Multilinear Functions (11).

Evaluation of Ph.D. Theses

1. Yael Moscowitz, Weizmann Institute, Rehovot, Israel, 1997.
2. Olivier Bournez, ENS Lyon, France, 1999.
3. Marius Bozga, UJF Grenoble, France, 1999.
4. Ansgar Fehnker, Univ. of Nijmegen, Netherlands, 2002.
5. Madhusudan Parthasarathy, Chennai Inst. of Technology, Chennai, India, 2002.
6. Ralf Huuck, University of Kiel, Germany, 2003.
7. Gerd Behrmann, Aalborg University, Denmark, 2004.
8. Antoine Girard, INPG, Grenoble, France, 2004.
9. Jim Kapinski, Carnegie-Mellon University, Pittsburgh, USA, 2004.
10. Sid-Ahmad Attiya, INPG, Grenoble, France, 2005.
11. Yang Shaofa, National University of Singapore, 2006.
12. Thomas Chaitin, University of Rennes, 2006.
13. Emmanuelle Encrenaz, Paris 6 (habilitation), 2007.
14. Jacob Illum Rasmussen, Aalborg University, Denmark, 2007.
15. Franck Cassez, Nantes (habilitation), 2007.
16. Nishant Sinha, Carnegie-Mellon university, Pittsburgh, USA, 2007.

17. Olga Grinschtein, Uppsala, Sweden, 2008.
18. Erik Saule, INPG Grenoble, 2008.
19. Samuel Drulhe, UJF Grenoble, 2008.
20. Federico Mari, Sapienza University, Rome, 2009.
21. Aurelien Rizk, University Paris 7, 2011.
22. Peter Niebert, University of Marseille (habilitation), 2011
23. Hans-Jörg Peter, Saarbrücken University, 2012.
24. Janusz Malinowski, University of Marseille, 2012.
25. Hua Mao, Aalborg University, Denmark, 2013.
26. Antoine Girard, University of Grenoble (habilitation), 2013.
27. Gregor Goessler, University of Grenoble (habilitation), 2014.
28. Nicolas Mobilia, University of Grenoble, 2015.
29. Goran Frehse, University of Grenoble (habilitation), 2016.
30. Yoann Geoffroy, University of Grenoble, 2016.
31. Ramanathan Rajendiran, National University of Singapore, 2017.

Projects

- 1992 – 1994: AFIRST (French-Israeli cooperation) project on hybrid systems with Weizmann Institute.
- 1993 – 1996: Coordinator of an NSF/Esprit network HYBRID-EC-US on hybrid systems, participants: Verimag, IRISA, Lund and Lyngby.
- 1995 – 1997: Coordinator of an INTAS project on hybrid systems (Verimag, Padova and the IPPI intitute of the Russian Academy of Science).
- 1997 – 1998: Contract with the EDF on modeling hybrid systems (300,000 FF).
- 1997 – 2000: Coordinator the *Esprit/LTR project 26270 VHS (Verification of Hybrid Systems)*, with the participation of UJF-Verimag, Dortmund, Nijmegen, Aalborg-Brics, Kiel, INPG-LAG, Weizmann, CWI, Ghent, Uppsala, ETH-Zurich, Nylstar SA, Sidmar, Krupp-Uhde. Overall budget: 930,000 Euro (290,000 Euro for Verimag).
- 1998 – 2000: AFIRST (French-Israeli cooperation) project on modeling of industrial plants with Technion and Weizmann Institute (200,000 FF).
- 2002 – 2005: Coordinator of the project *IST 33520 CC (Control and Computation)* with the participation of INPG-Verimag, ETHZ, Parades, Lund, CWI, Sienna, EDF and ABB. Overall budget 1.48 MEuro (472 KEuro for Verimag).

- 2002 – 2005: Scientific coordinator of the project *IST 35304 AMETIST (Advanced Methods for Real-Time Systems)* with the participation of Nijmegen, UJF-Verimag, Aalborg, Twente, Marseille, Bosch, Axxom, Cybernetix and Terma. Overall budget 2 MEuro (255 KEuro for Verimag).
- 2002 – 2004: Research Grant from *Intel*, Combining Timing Analysis and Formal Verification, 100K\$.
- 2003 – 2006: participation in the project *IST 50720 PROSYD (Property-based System Design)* together with IBM, Infineon, ST microelectronics, Graz, Trento, Weizmann. Budget for Verimag: 300KEuro.
- 2006 – 2008: participation in the RNTL project *Decide!* with ILOG SA about the use of constraint solvers for verifying business rules. Budget for Verimag: 200KEuro.
- 2007 – 2008: French-Israeli project *Computational Modeling of Incomplete Biological Regulatory Networks* with Weizmann Institute. Budget for Verimag: 50KEuro.
- 2007 – 2011: Minalogic project *Ahole* with ST, CEA-LETI, Thales and CWS. Role in the project: *Programming Environment for Stream-Processing applications and Scheduling on Multicore Architecture*. Budget for Verimag: 830KEuro
- 2010-2011: France-Canada Research Fund, *Verification of Analog Circuits* with UBC Vancouver.
- 2010-2012: P2012 Initiative, Grenoble: Deploying Streaming Programs on Multi-Core Computers, 50KEuro
- 2010-2013: participation in the ANR project, *Syne2arti* on synthetic biology with INRIA Rocquencourt. Budget for Verimag: 135KEuro
- 2011-2014: participation in the ANR project, *Equinocs* on entropy of computational models, with LIAFA, LIGM and LACL. Budget for Verimag: 70KEuro
- 2013-2017: participation in the ANR project, *Cadmidia* on the metabolism of Cadmium, with TIMC and LBFA. Budget for Verimag: 85KEuro
- 2014-2017: participation in the European Defense Agency project, *Mistral* on monitoring AMS assertions with Austrian Institute of Technology and Easii-IC. Budget for Verimag: 138KEuro
- 2015-2017: Nano2017 project with ST Microelectronics, Noise propagation in analog circuits. Budget: 260KEuro.
- 2012-2017: Various industrial contracts with Atrenta, Mentor Graphics, Kalray, United Technologies, Toyota, Bosch and Easii-ic.
- 2018-2019: UGA IDEX project: CyberPhysical Data Mining for Predictive Maintenance.
- 2018-2021: INSERM Plan Cancer project: MODYLAN modeling Acute Myeloid Leukemia
- 2018-2021: UGE IDEX inter-disciplinary project: SYMER, Epigenetics and Metabolism.

Project Evaluations

- Member of the evaluation committee of the ANR program *SESUR* on safety and security (2007).
- Evaluation of research proposals and researchers for: Israel Science Foundation, McArthur Foundation, ETH Zurich, National University of Singapore, University of Oldenburg, InNaBioSante Foundation, Canadian Science Foundation, Technion, Microsoft Research, Dutch Science Foundation, Austrian Science Fund, Swiss National Science Foundation, Indian Institute of Technology Bangalore, Israel-India Science Foundation, US National Science Foundation (NSF), Singapore Education Ministry, INRIA, ANR, CHIST-ERA, Belgian Science Foundation (FNRS), ERC, US-Israel Binational Science Foundation, Oxford University.

Publications

(J): Journal Articles and Handbook Chapters

1. B. Delyon and O. Maler, On the Effects of Noise and Speed on Computations, *Theoretical Computer Science* 129, 279-291, 1994.
2. O. Maler and A. Pnueli, On the Learnability of Infinitary Regular Sets, *Information and Computation* 118, 316-326, 1995.
3. A. Asarin, O. Maler and A. Pnueli, On the Analysis of Dynamical Systems having Piecewise-Constant Derivatives, *Theoretical Computer Science* 138, 35-65, 1995.
4. O. Maler, A Decomposition Theorem for Probabilistic Transition Systems, *Theoretical Computer Science* 145, 391-396, 1995.
5. O. Maler and L. Staiger, On Syntactic Congruences for ω -Languages, *Theoretical Computer Science* 183, 93-112, 1997.
6. E. Asarin and O. Maler, Achilles and the Tortoise Climbing Up the Arithmetical Hierarchy, *Journal of Computers and Systems Science* 57, 389-398, 1998.
7. E. Asarin, O. Bournez, T. Dang, O. Maler and A. Pnueli, Effective Synthesis of Switching Controllers for Linear Systems, *Proceedings of the IEEE* 88, 1011-1025, 2000.
8. A. Bouajjani, J. Esparza, A. Finkel, O. Maler, P. Rossmanith, B. Willems, and P. Wolper, An Efficient Automata Approach to some Problems on Context-free Grammars, *Information Processing Letters* 74, 221-227, 2000.
9. Y. Kesten, O. Maler, M. Marcus, A. Pnueli and E. Shahar, Symbolic Model Checking with Rich Assertion Languages, *Theoretical Computer Science* 256, 93-112, 2001.
10. O. Maler, Guest Editorial: Verification of Hybrid Systems, *European Journal of Control* 7, 357-365, 2001.
11. E. Asarin, P. Caspi and O. Maler, Timed Regular Expressions, *Journal of the ACM* 49, 172-206, 2002.
12. O. Maler, Control from Computer Science, *Annual Reviews in Control* 26, 175-187, 2002.
13. P. Caspi and O. Maler, From Control Loops to Real-Time Programs, *Handbook of Networked and Embedded Systems*, 395-418, Birkhauser, 2005.
14. Y. Abdeddaim, E. Asarin and O. Maler Scheduling with Timed Automata, *Theoretical Computer Science* 354, 272-300, 2006.
15. O. Maler, On Optimal and Reasonable Control in the Presence of Adversaries, *Annual Reviews in Control* 31, 1-15, 2007.

16. O. Maler, A. Pnueli and D. Nickovic, Checking Temporal Properties of Discrete, Timed and Continuous Behaviors, *Pillars of Computer Science. Essays Dedicated to Boris (Boaz) Trakhtenbrot on the Occasion of His 85th Birthday*, LNCS 4800, 2008.
17. O. Maler, On the Krohn-Rhodes Cascaded Decomposition Theorem, *Time for Verification: Essays in Memory of Amir Pnueli*, 2010.
18. T. Dang, C. Le Guernic, O. Maler, Computing Reachable States for Nonlinear Biological Models, *Theoretical Computer Science* 412, 2095-2107, 2011.
19. A. Donzé, E. Fanchon, L.M. Gattepaille, O. Maler and Ph. Tracqui, Robustness Analysis and Behavior Discrimination in Enzymatic Reaction Networks, *PLoS One* 6(9), 2011.
20. S. Saidi, P. Tendulkar, T. Lepley and O. Maler, Optimizing Explicit Data Transfers for Data Parallel Applications on the Cell Architecture, *ACM Transactions on Architecture and Code Optimization* 8(4), 1544-3566, 2012.
21. O. Maler, and D. Nickovic, Monitoring Properties of Analog and Mixed-Signal Designs, *Software Tools for Technology Transfer*, 2013.
22. S. Stoma, A. Donze, F. Bertaux, O. Maler and G. Batt, STL-based analysis of TRAIL-induced apoptosis challenges the notion of type I/type II cell line classification, *PLoS Comp. Biology*, 2013.
23. S. Saidi, P. Tendulkar, T. Lepley, O. Maler, Optimizing Two-Dimensional DMA Transfers for Scratchpad Based MPSoCs Platforms, *Microprocessors and Microsystems - Embedded Hardware Design* 37, 848-857, 2013.
24. O. Maler, I.E. Mens, Learning Regular Languages over Large Ordered Alphabets, *Logical Methods in Computer Science*, 2015.
25. E Bartocci, J. Deshmukh, A. Donze, G. Fainekos, O. Maler, D. Nickovic, S. Sankaranarayanan, Monitoring Cyber-Physical Systems, in Handbook of Runtime Verification, to appear.

Refereed Conference Articles (already published in journals)

1. O. Maler and A. Pnueli, On the Learnability of Infinitary Regular Sets, *Proc. 4th Annual Workshop on Computational Learning Theory*, 128-136, Morgan Kaufman, 1991.
2. B. Delyon and O. Maler, On Fault-Tolerant Symbolic Computations, *FTRTFT*, LNCS 571, 259-269, 1992.
3. O. Maler, A Decomposition Theorem for Probabilistic Transition Systems, *STACS*, 323-332, LNCS 665, 1993.
4. O. Maler and L. Staiger, On Syntactic Congruences for ω -Languages, *STACS*, 586-594, LNCS 665 , 1993.
5. O. Maler and A. Pnueli, Reachability Analysis of Planar Multi-Linear Systems, *CAV*, LNCS 697, 194-209, 1993.
6. E. Asarin and O. Maler, On some Relations between Dynamical Systems and Transition Systems, *ICALP*, 59-72, LNCS 820, 1994.

7. E. Asarin and O. Maler, Achilles and the Tortoise Climbing Up the Arithmetical Hierarchy, *FST/TCS*, 471-483, LNCS 1026, 1995.
8. Y. Kesten, O. Maler, M. Marcus, A. Pnueli and E. Shahar, Symbolic Model Checking with Rich Assertion Languages, *CAV*, 424-435, LNCS 1254, 1997.
9. E. Asarin, O. Maler and P. Caspi, A Kleene Theorem for Timed Automata, *LICS*, 160-171, 1997.
10. O. Maler, Control from Computer Science, *IFAC Symposium Nonlinear Control (NOLCOS'01)*, Elsevier, 2001.
11. Y. Abdeddaim, O. Maler, Job-Shop Scheduling using Timed Automata, *CAV*, 478-492, LNCS 2102, 2001.
12. Y. Abdeddaim, E. Asarin and O. Maler, On Optimal Scheduling under Uncertainty, *TACAS* 240-255, LNCS 2619, 2003.
13. Y. Abdeddaim, A. Kerbaa and O. Maler, Task Graph Scheduling using Timed Automata *Int. Parallel and Distributed Processing Symposium (IPDPS)*, 237-245, 2003.
14. O. Maler and D. Nickovic, Monitoring Temporal Properties of Continuous Signals, *FOR-MATS/FTRTFT*, 152-166, LNCS 3253, 2004.
15. O. Maler, On Optimal and Sub-optimal Control in the Presence of Adversaries, *WODES*, 1-12, 2004.
16. P. Caspi and O. Maler, On the Implementation of Control Loops by Software, *CACSD*, 2006.
17. T. Dang, C. Le Guernic and O. Maler, Computing Reachable States for Nonlinear Biological Models, *CMSB'09*, 2009.
18. S. Saidi, P. Tendulkar, T. Lepley and O. Maler, Optimizing Explicit Data Transfers for Data Parallel Applications on the Cell Architecture, *HiPeac*, 2012.
19. S. Saidi, P. Tendulkar, T. Lepley, O. Maler, Optimal 2D Data Partitioning for DMA Transfers on MPSoCs, *DSD* 2012.
20. O. Maler, I.E. Mens, Learning Regular Languages over Large Alphabets, *TACAS*, 2014.

(C): Refereed Conference Articles (not published in journals)

1. O. Maler and A. Pnueli, Tight Bounds on the Complexity of Cascaded Decomposition of Automata, *FOCS*, 672-682, IEEE Press, 1990.
2. O. Maler, Z. Manna, and A. Pnueli, From Timed to Hybrid Systems, *Real-Time: Theory in Practice*, 447-484, LNCS 600, 1992.
3. O. Maler, A. Pnueli and J. Sifakis, On the Synthesis of Discrete Controllers for Timed Systems, *STACS*, 229-242, LNCS 900, 1995.
4. E. Asarin, O. Maler and A. Pnueli, Symbolic Controller Synthesis for Discrete and Timed Systems, *Hybrid Systems II*, 1-20, LNCS 999, 1995.

5. O. Maler and A. Pnueli, Timing Analysis of Asynchronous Circuits using Timed Automata, *CHARME*, 189-205, LNCS 987, 1995.
6. O. Maler and S. Yovine, Hardware Timing Verification using KRONOS, *7th Isr. Conf. on Computer-based Systems and Software Engineering*, 23-29, IEEE Press, 1996.
7. E. Asarin, M. Bozga, A. Kerbrat, O. Maler, A. Pnueli and A. Rasse, Data-Structures for the Verification of Timed Automata, *Hybrid and Real-Time Systems (HART)*, 346-360, LNCS 1201, 1997.
8. M. Bozga, O. Maler, A. Pnueli and S. Yovine, Some Progress in the Symbolic Verification of Timed Automata, *CAV*, 179-190, LNCS 1254, 1997.
9. A. Bouajjani, J. Esparza and O. Maler, Reachability Analysis of Pushdown Automata: Application to Model-Checking, *CONCUR*, 135-150, LNCS 1243, 1997.
10. T. Dang, O. Maler, Reachability Analysis via Face Lifting, *HSCC*, 96-109, LNCS 1386, 1998.
11. E. Asarin, O. Maler and A. Pnueli, On Discretization of Delays in Timed Automata and Digital Circuits, *CONCUR*, 470-484, LNCS 1466, 1998.
12. E. Asarin, O. Maler, A. Pnueli and J. Sifakis, Controller Synthesis for Timed Automata, *IFAC Symp. on Systems, Structure and Control*, 469-474, Elsevier, 1998.
13. O. Maler, A Unified Approach for Studying Discrete and Continuous Dynamical Systems, *CDC*, 2083-2088, IEEE, 1998.
14. M. Bozga, C. Daws, O. Maler, A. Olivero, S. Tripakis and S. Yovine Kronos: A Model-Checking Tool for Real-Time Systems, *CAV*, 546-550, LNCS 1427, 1998.
15. E. Asarin and O. Maler, As Soon as Possible: Time Optimal Control for Timed Automata, *HSCC*, 19-30, LNCS 1569, 1999.
16. O. Bournez, O. Maler and A. Pnueli, Orthogonal Polyhedra: Representation and Computation, *HSCC*, 46-60, LNCS 1569, 1999.
17. M. Bozga and O. Maler, On the Representation of Probabilities over Structured Domains, *CAV*, 261-273, LNCS 1633, 1999.
18. M. Bozga, O. Maler and S. Tripakis, Efficient Verification of Timed Automata using Dense and Discrete Time Semantics, *CHARME*, 125-141, LNCS 1703, 1999.
19. E. Asarin, O. Bournez, T. Dang and O. Maler, Reachability Analysis of Piecewise-Linear Dynamical Systems, *HSCC*, 20-31, LNCS 1790, 2000.
20. O. Bournez and O. Maler, On the Representation of Timed Polyhedra, *ICALP*, 793-807, LNCS 1853, 2000.
21. E. Asarin, S. Bansal, T. Dang, B. Espiau and O. Maler, On Hybrid Control of Under-actuated Mechanical Systems, *HSCC*, 89-104, LNCS 2034, 2001.
22. Y. Abdeddaim and O. Maler, Preemptive Job-Shop Scheduling using Stopwatch Automata, *TACAS*, 113-126, LNCS 2280, 2002.

23. M. Bozga, H. Jianmin, O. Maler and S. Yovine, Verification of Asynchronous Circuits using Timed Automata, *Workshop on Theory and Practice of Timed Systems (TPTS)*, 2002.
24. B. Krogh, O. Maler and M. Mahfoudh, On Control with Bounded Computational Resources, *FTRTFT*, 147-162, LNCS 2469, 2002.
25. P. Niebert, M. Mahfoudh, E. Asarin, M. Bozga, N. Jain and O. Maler, Verification of Timed Automata via Satisfiability Checking, *FTRTFT*, 225-243, LNCS 2469, 2002.
26. B. Krogh, J. Kapinski, O. Maler and O. Stursberg, On Systematic Simulation of Open Continuous Systems, *HSCC*, 283-297, LNCS 2623, 2003.
27. R. Ben Salah, M. Bozga and O. Maler, On Timing Analysis of Combinational Circuits, *FORMATS*, 204 - 219, LNCS 2791, 2003.
28. O. Maler and A. Pnueli, On Recognizable Timed Languages, *FOSSACS*, 348-362, LNCS 2987, 2004.
29. S. Cotton, E. Asarin, O. Maler and P. Niebert, Some Progress in Satisfiability Checking for Difference Logic, *FORMATS/FTRTFT*, 263-276, LNCS 3253, 2004.
30. O. Maler and D. Nickovic, Monitoring Temporal Properties of Continuous Signals, *FORMATS/FTRTFT*, 152-166, LNCS 3253, 2004.
31. T. Dang, A. Donze and O. Maler, Verification of Analog and Mixed Signal Circuits using Hybrid Systems Techniques, *FMCAD*, 21-36, LNCS 3312, 2004.
32. M. Bozga, A. Kerbaa and O. Maler, Scheduling Acyclic Branching Programs on Parallel Machines *RTSS*, 208-217, IEEE Press, 2004.
33. G. Frehse, B. Krogh, R. Rutenbar and O. Maler, Time Domain Verification of Oscillator Circuit Properties, *Workshop on Formal Verification of Analog Circuits (FAC)*, 1-13, 2005.
34. O. Maler, D. Nickovic and A. Pnueli, Real Time Temporal Logic: Past, Present, Future, *FORMATS*, 2-16, LNCS 3829, 2005.
35. A. Girard, C. Le Guernic and O. Maler, Efficient Computation of Reachable Sets of Linear Time-Invariant Systems with Inputs, *HSCC*, 257-271, LNCS 3927, 2006.
36. E. Asarin, T. Dang, G. Frehse, A. Girard, C. Le Guernic and O. Maler, Recent Progress in Continuous and Hybrid Reachability Analysis, *CACSD*, 2006.
37. S. Cotton and O. Maler, Fast and Flexible Difference Logic Propagation for DPLL(T), *SAT'06*, 170-183, LNCS 4121, 2006.
38. R. Ben Salah, M. Bozga and O. Maler, On Interleaving in Timed Automata, *CONCUR'06*, 465-476, LNCS 4137, 2006.
39. O. Maler, D. Nickovic and A. Pnueli, From MITL to Timed Automata, *FORMATS'06*, 274-289, LNCS 4202, 2006.
40. A. Donze and O. Maler, Systematic Simulation using Sensitivity Analysis, *HSCC'07*, 174-189, LNCS 4416, 2007.

41. O. Maler, D. Nickovic and A. Pnueli, On Synthesizing Controllers from Bounded-Response Properties, *CAV'07*, 95-107, LNCS 4590, 2007.
42. G. Batt, R. Ben Salah and O. Maler, On Timed Models of Gene Networks, *FORMATS'07*, 38-52, LNCS 4763, 2007.
43. D. Nickovic and O. Maler, AMT: a Property-based Monitoring Tool for Analog Systems, *FORMATS'07*, 304-319, LNCS 4763, 2007.
44. O. Maler and G. Batt, Approximating Continuous Systems by Timed Automata, *FMSB'08*, 77-89, LNCS 5054, 2008.
45. A. Degorre, O. Maler, On Scheduling Policies for Streams of Structured Jobs, *FORMATS'08*, 141-154, LNCS 5215, , 2008.
46. T. Dang, A. Donze, O. Maler, N. Shalev, Sensitive State Space Exploration, *CDC'08*, 2008.
47. R. Alur, A. Degorre, O. Maler and G. Weiss, On Omega-Languages Defined by Mean-Payoff Conditions, *FOSSACS'09*, 333-347, LNCS 5504, , 2009.
48. R. Ben Salah, M. Bozga and O. Maler, Compositional Timing Analysis, *EMSOFT*, 2009.
49. T. Dang, O. Maler and R. Testylier, Accurate Hybridization of Nonlinear Systems, *HSCC*, 2010.
50. J. Legriel, C. Le Guernic, S. Cotton and O. Maler, Approximating the Pareto Front of Multi-Criteria Optimization Problems, *TACAS*, 2010.
51. A. Donze, O. Maler, Robust Satisfiability of Temporal Logic over Real-Valued Signals, *FORMATS*, 2010.
52. E. Asarin. T. Dang, O. Maler and R. Testylier, Using Redundant Constraints for Refinement, *ATVA*, 2010.
53. O. Maler, K. Larsen and B. Krogh, On Zone-Based Analysis of Duration Probabilistic Automata, *Infinity*, 2010.
54. G. Frehse, C. Le Guernic, A. Donze, S. Cotton, R. Ray, O. Lebeltel, R. Ripado, A. Girard, T. Dang, O. Maler, SpaceEx: Scalable Verification of Hybrid Systems, *CAV* 2011.
55. S. Cotton, J. Legriel, O. Maler, On Universal Search Strategies for Multi-Criteria Optimization Using Weighted Sums, *CEC* 2011.
56. J. Legriel, O. Maler, Meeting Deadlines Cheaply, *ECRTS* 2011.
57. S. Cotton, J. Legriel, S. Saidi, O. Maler, Multi-Criteria Optimization for Mapping Programs to Multi-Processors, *SIES* 2011.
58. J.-F. Kempf, M. Bozga, O. Maler, Performance Evaluation of Schedulers in a Probabilistic Setting, *FORMATS* 2011.
59. O. Maler, On Under-Determined Dynamical Systems, *EMSOFT* 2011.
60. E. Asarin, A. Donze, O. Maler, D. Nickovic, Parametric Identification of Temporal Properties, *RV* 2011.

61. A. Donzé, O. Maler, E. Bartocci, D. Niccovic, R. Grosu, S. Smolka, On Temporal Logic and Signal Processing, *ATVA*, 2012.
62. J.-F. Kempf, M. Bozga, O. Maler, As Soon as Probable: Optimal Scheduling under Stochastic Uncertainty, *TACAS*, 2012.
63. A. Donze, T. Ferrere, O. Maler, Efficient Robust Monitoring for STL, *CAV*, 2013.
64. P. Tendulkar, P. Poplavko, O. Maler, Symmetry Breaking for Multi-Criteria Mapping and Scheduling on Multicores, *FORMATS* 2013.
65. O. Maler, A. Halasz, O. Lebeltel, O. Maler, Exploring Synthetic Mass Action Models, *Proc. HSB*, 2015.
66. O. Maler, Algorithmic Verification of Continuous and Hybrid Systems, *Infinity*, 2013.
67. O. Maler, The Unmet Challenge of Timed Systems, *From Program to Systems*, 2014.
68. J.-F. Kempf, O. Lebeltel, O. Maler, Formal and Informal Methods for Multi-Core Design Space Exploration, *QAPL*, 2014.
69. D. Ulus, T. Ferrere, E. Asarin, O. Maler, Timed Pattern Matching, *FORMATS*, 2014.
70. P. Tendulkar, P. Poplavko, I. Galanommatis, O. Maler, Many-Core Scheduling of Data Parallel Applications using SMT Solvers, *DSD* 2014.
71. P. Tendulkar, P. Poplavko, O. Maler, Pipelined Scheduling of Acyclic SDF Graphs using SMT Solvers, *IDEA* 2015.
72. T. Ferrere, O. Maler, D. Ulus, D. Nickovic, Measuring with Timed Patterns, *CAV*, 2015.
73. J. Deshmukh, X. Jin, J. Kapinski, O. Maler, Stochastic Local Search for Falsification of Hybrid Systems, *ATVA*, 2015.
74. T. Ferrere, O. Maler, D. Nickovic, Trace Diagnostics using Temporal Implicants, *ATVA* 2015.
75. J. Lanik, J. Legriel, E. Piriou, E. Viaud, F. Rahim, O. Maler, S. Rahim, Reducing Power with Activity Trigger Analysis, *MEMOCODE*, 2015.
76. J. Lanik, O. Maler, On Switching Aware Synthesis for Combinational Circuits, *HVC*, 2015.
77. D. Ulus, T. Ferrere, E. Asarin, O. Maler, Online Timed Pattern Matching using Derivatives, *TACAS*, 2016.
78. O. Maler, Some Thoughts on Runtime Verification, *RV*, 2016.
79. O. Maler, A. Srivastav, Double Archive Pareto Local Search, *SSCI*, 2016.
80. O. Maler, I.E. Mens, A Generic Algorithm for Learning Symbolic Automata from Membership Queries, Larsen Festschrift, 2017.
81. A. Bakhirkin, T. Ferrere, O. Maler, D. Ulus, On the Quantitative Semantics of Signal Regular Expressions over Real-Valued Signals, *FORMATS* 2017.

82. E. Asarin, O. Maler, D. Nickovic, D. Ulus, Combining the Temporal and Epistemic Dimensions for MTL Monitoring, FORMATS 2017.
83. D. Nickovic, O. Lebeltel, O. Maler, T. Ferrere, D. Ulus, AMT 2.0: Qualitative and Quantitative Trace Analysis with Extended Signal Temporal Logic, TACAS 2018.
84. A. Bakhirkin, T. Ferrere, O. Maler, Efficient Parametric Identification for STL, HSCC 2018.
85. O. Maler, D. Ulus, Specifying Timed Patterns using Temporal Logic, HSCC 2018.

(B): Books and Proceedings

1. O. Maler, *At least now* (Poems), Out, Haifa, 1978. (in Hebrew)
2. O. Maler, E. Shapiro and Z. Schertz, *Hebrew Prolog for Beginners*, Ramot, Tel-Aviv, 1988. (in Hebrew)
3. A. Bouajjani and O. Maler (Eds.), *Proc. of the European Workshop on Real-Time and Hybrid Systems*, Grenoble, France 1995.
4. O. Maler (Ed.), *Hybrid and Real-Time Systems, International Workshop HART'97*, Grenoble, LNCS 1201, Springer, 1997.
5. O. Maler (Ed.), *Verification of Hybrid Systems*, Hermes, 2001.
6. E. Asarin, O. Maler and S. Yovine (Eds.), *Theory and Practice of Timed Systems (TPTS'02)*, Grenoble, 2002.
7. O. Maler and A. Pnueli (Eds.), *Hybrid Systems: Computation and Control*, LNCS 2623, Springer , 2003.
8. O. Maler (Ed.), *Formal Verification of Analog Circuits (FAC)*, ENTCS 153:3, 1-78, 2005.
9. A. Bouajjani and O. Maler (Eds.), *Computer Aided Verification, 21st International Conference, CAV 2009*, Grenoble, LNCS 5643, Springer, 2009.
10. O. Maler, A. Halasz, T. Dang, C Piazza (Eds.), *Hybrid Sytstem Biology, HSB' 2013-2014*, LNBI 4699, 2015.

Software

- **d/dt:** Reachability Computation for Continuous and Hybrid Systems (T. Dang).
- **jat** and **jac**: Solvers for SAT and QBF (S. Cotton).
- **AMT:** Monitoring properties of analog signals (D. Nickovic).
- **BREACH:** Parameter-space exploration using sensitivity (A. Donze).
- **TCA:** Analysis of timed circuits (R. Ben Salah and M. Bozga).
- **SPACEEX, THE STATE-SPACE EXPLORER:** a new generation hybrid verification tool (G. Frehse et al.).

- DESIGN-SPACE EXPLORER: High-level performance evaluation (J.-F. Kempf and M. Bozga).
- STREAM EXPLORER: Deploying Data-Flow Streaming Application on Multi-Cores (P. Tendulkar and P. Poplavko).
- POPULUS: Exploring mass action dynamics (Ou. Maler and O. Lebeltel).