Using discrete controller synthesis for fault-tolerant distributed systems

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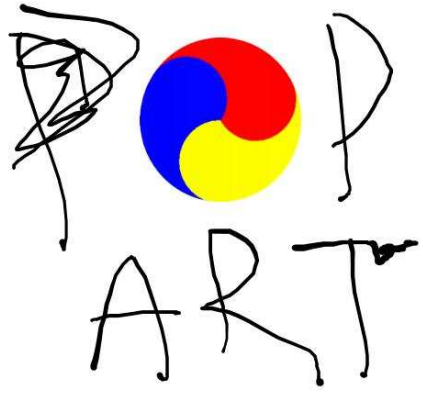

Motivations and context

Embedded systems (aeronautics, automotive, ...)

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- safe design using off-line validation
  → need for **formal models** e.g., transition systems
- safe execution with on-line fault recovery
  → need for **fault tolerance** e.g., recovery

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producing automatically a controller
enforcing fault-tolerance for a distributed system

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Using controller synthesis for fault-tolerance

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Using controller synthesis: find, if it exists,
the controller of the model enforcing the properties

$\longrightarrow$ synthesis of the correct reconfiguration controller

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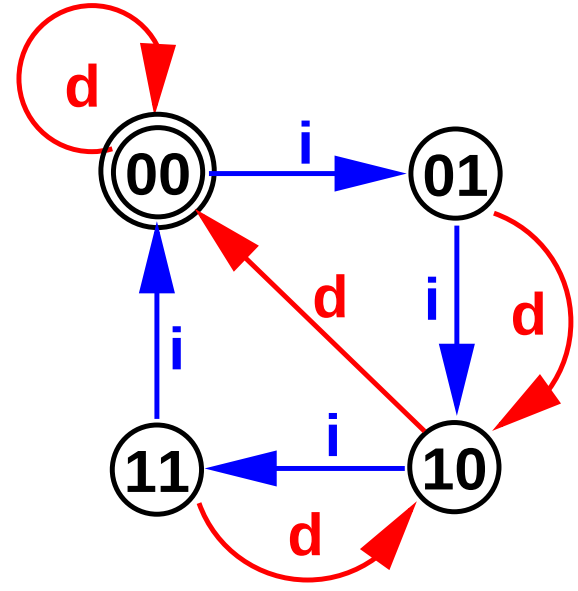
Discrete control synthesis

Purpose: *make* a property hold in the controlled system*!*

transition system:

all possible behaviours

(incl. bad ones)



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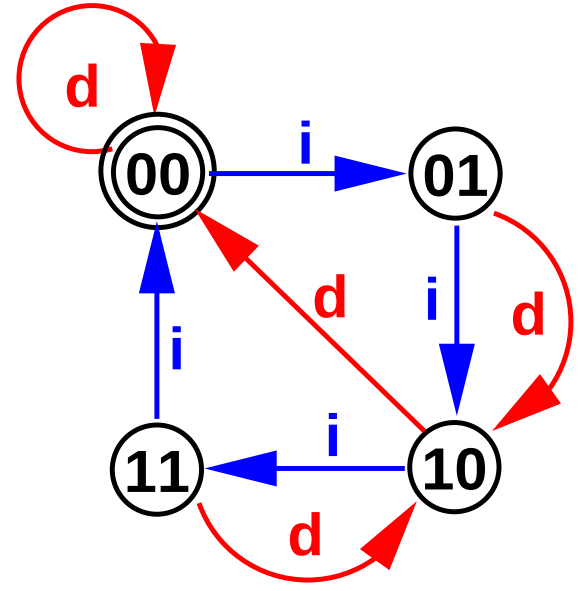

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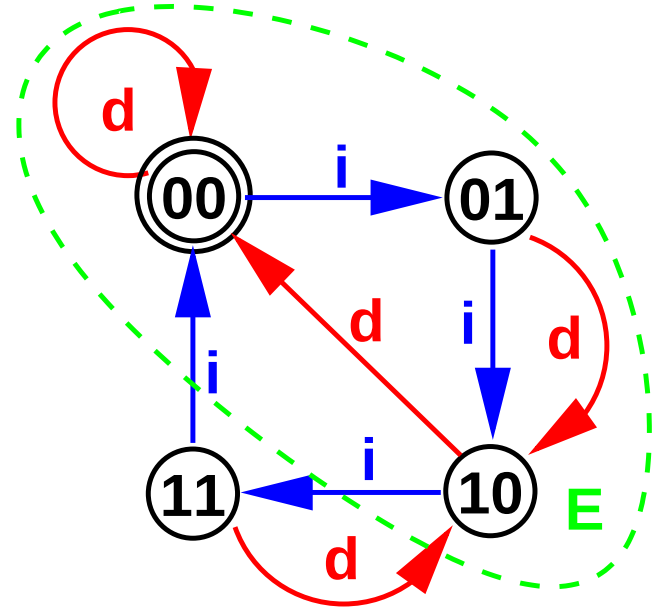

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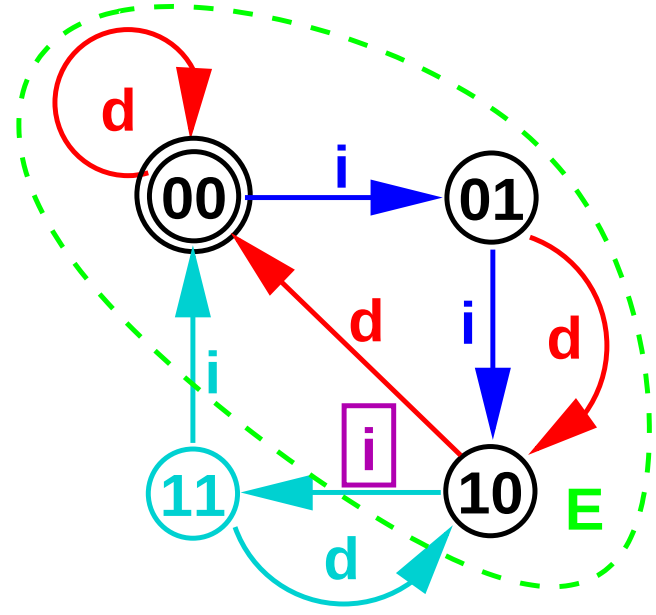
controller $\{ctrl\}=f(state, unctrl)$

e.g., *inhibit event* i *from state* 10



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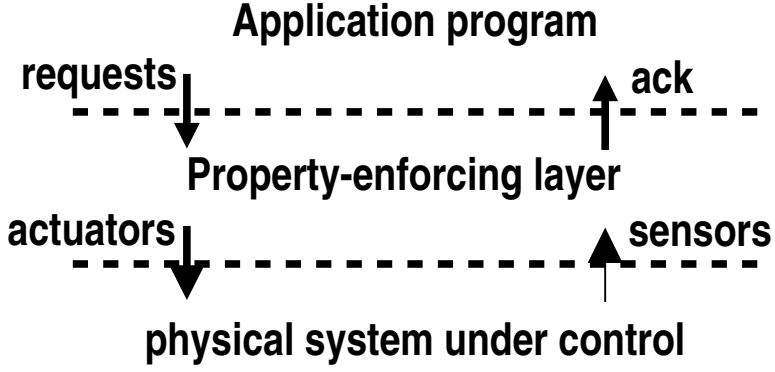

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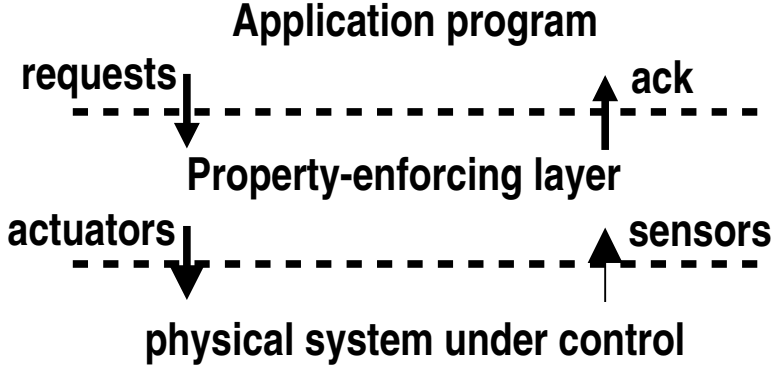

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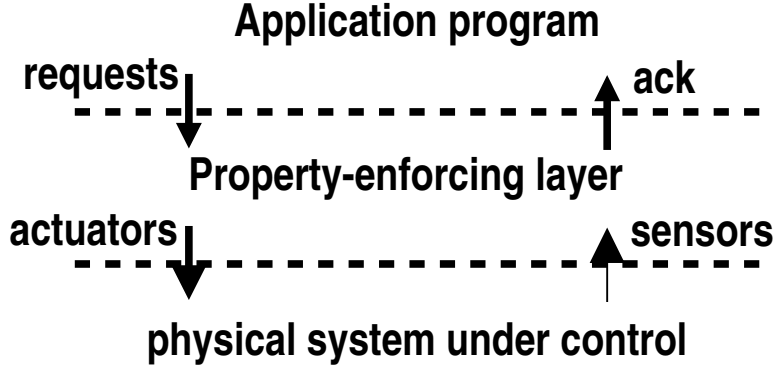


Automatic generation of property enforcing layers

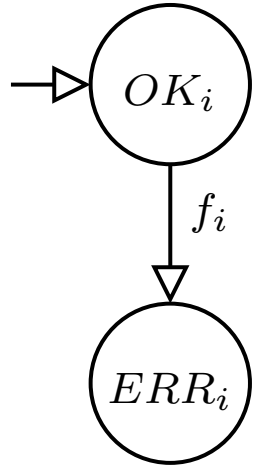
- correct control not just monitoring
- efficient synthesis (relatively) on prepared model

Architecture model

Local processor: fail-silent, permanent failure

multiple tasks, time-sharing; load are additive

quantitative bounds b_i (e.g., power, CPU load)



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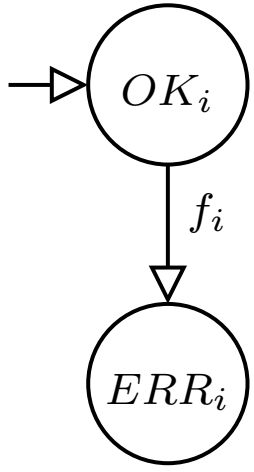

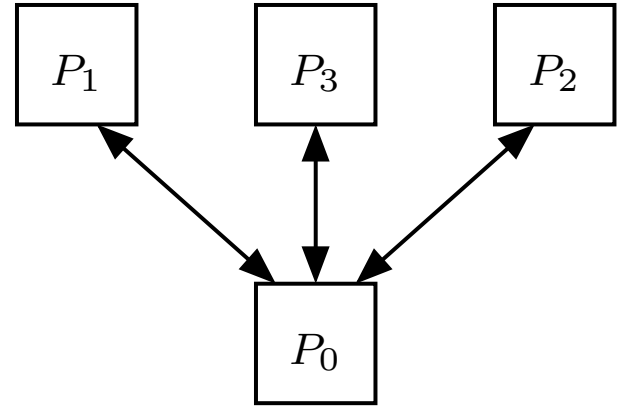

$\mathcal{S} = \{P_1, P_2, P_3\}$

Network model: *heterogeneous*

processor P_0 dedicated for control, failless

fully connected network, no communication failure

Environment or fault model

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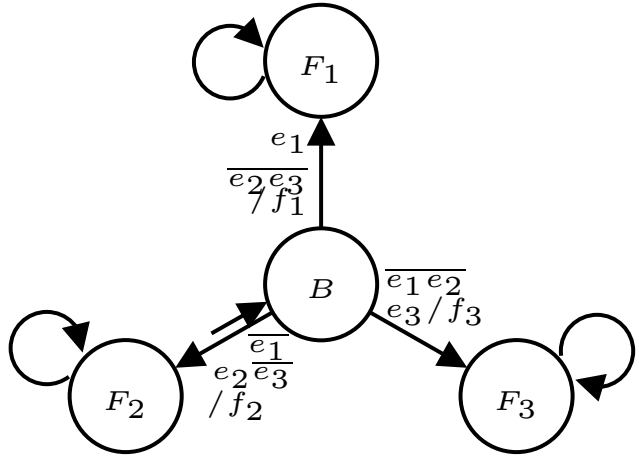

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(b) two failures possibly simultaneously

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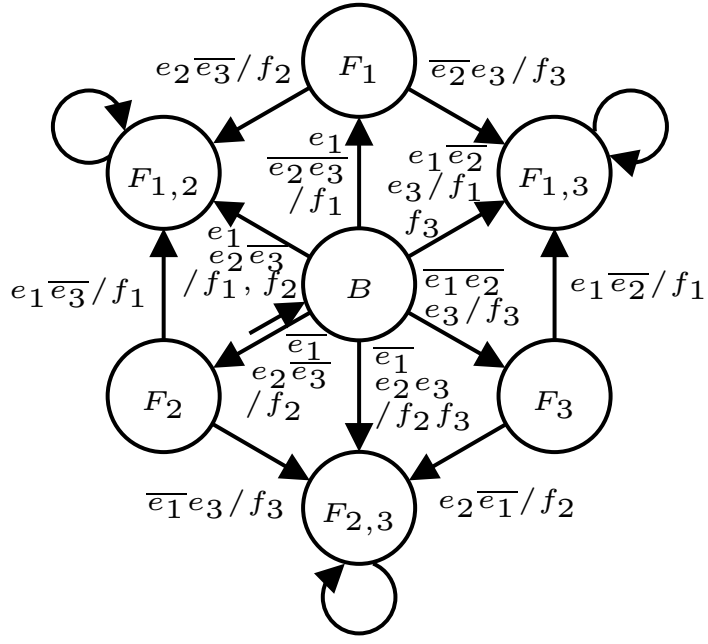

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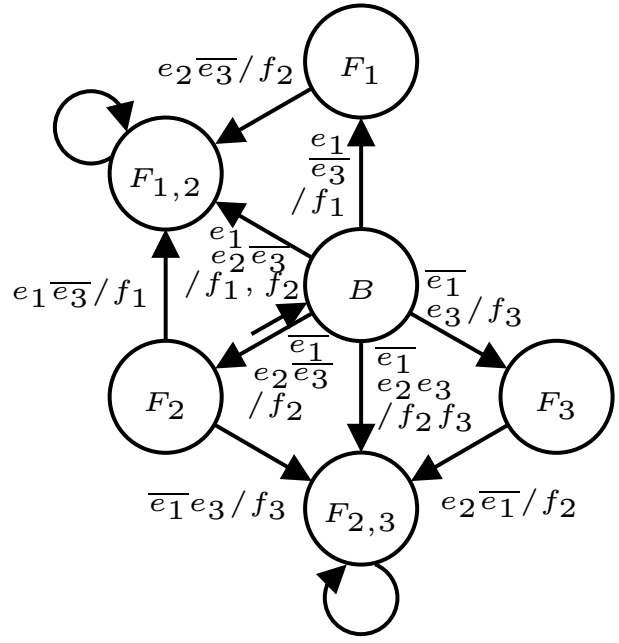
(c) other patterns e.g., not 1 and 3 together

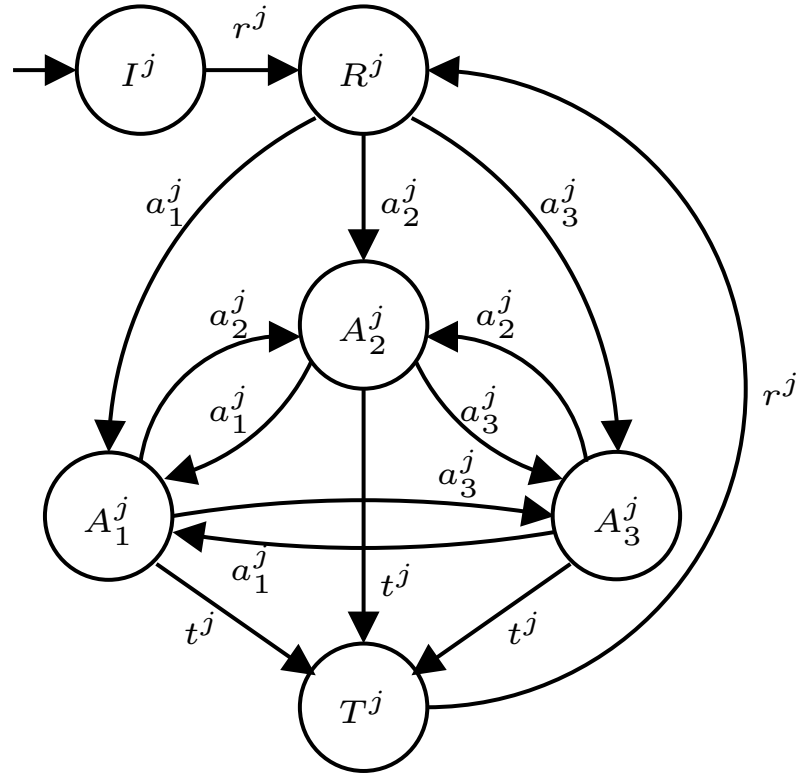
(c)



Task model (i)

Basic control structure pattern

task j, executable on 3 procs.



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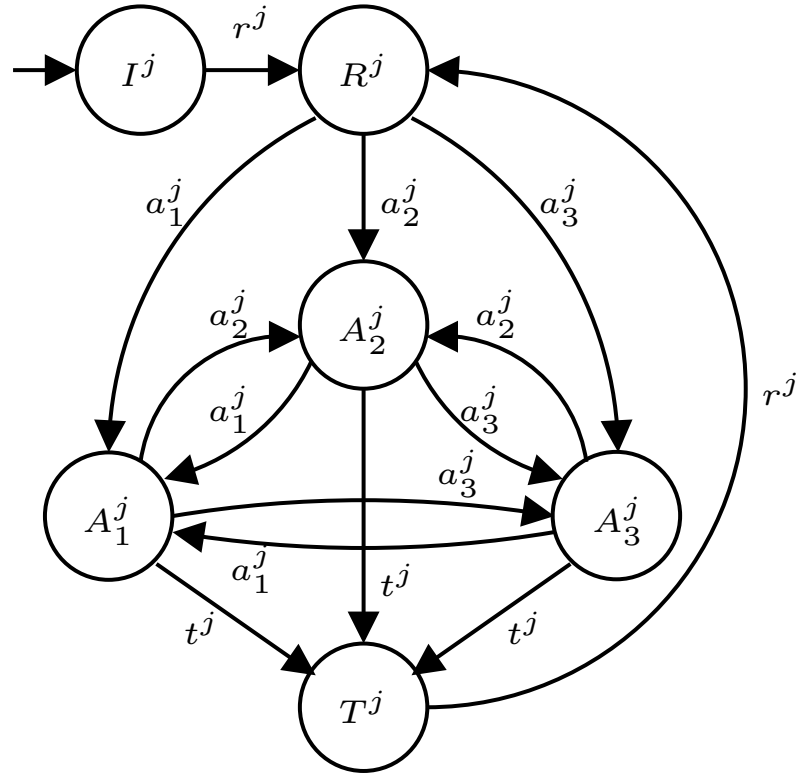

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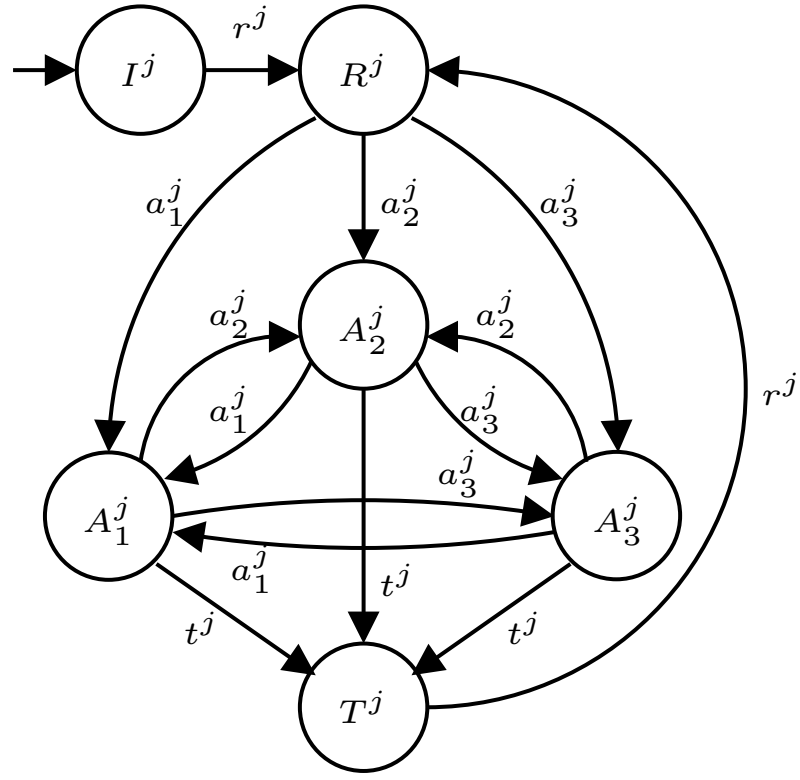
re-configuration: transition

(controllable) from A_i^j to A_k^j



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Power consumption		processor		
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task	T^1	4	4	2
	T^2	2	2	3
	T^3	2	3	4
bound		5	3	6

Task model (ii)

Quantitative characteristics: weights associated with states

- Execution time or CPU load required by each task
- Power consumption on a given processor
- Quality of the functionality (accuracy, depth of search, algorithm versions, ...)

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Tasks server: n tasks in parallel

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composition of costs e.g., addition:

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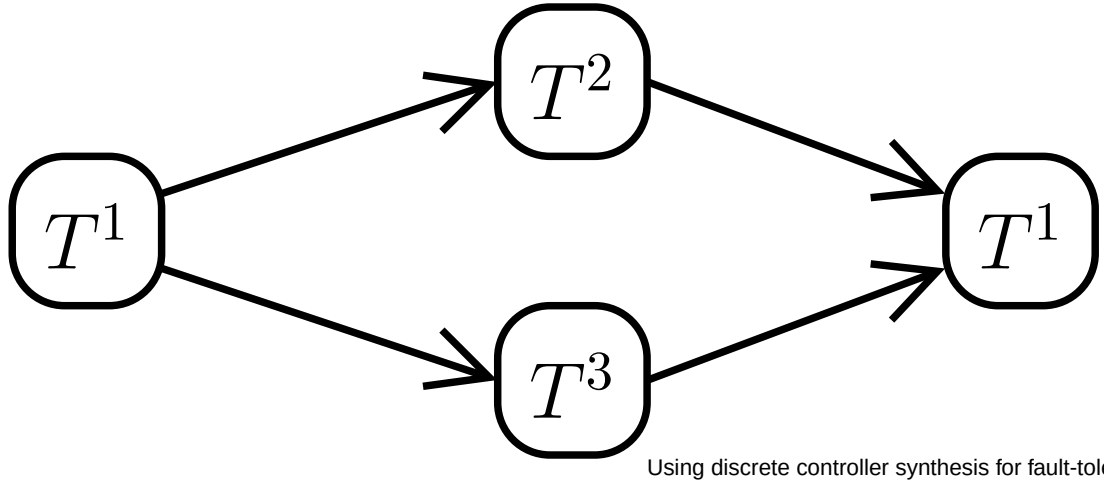
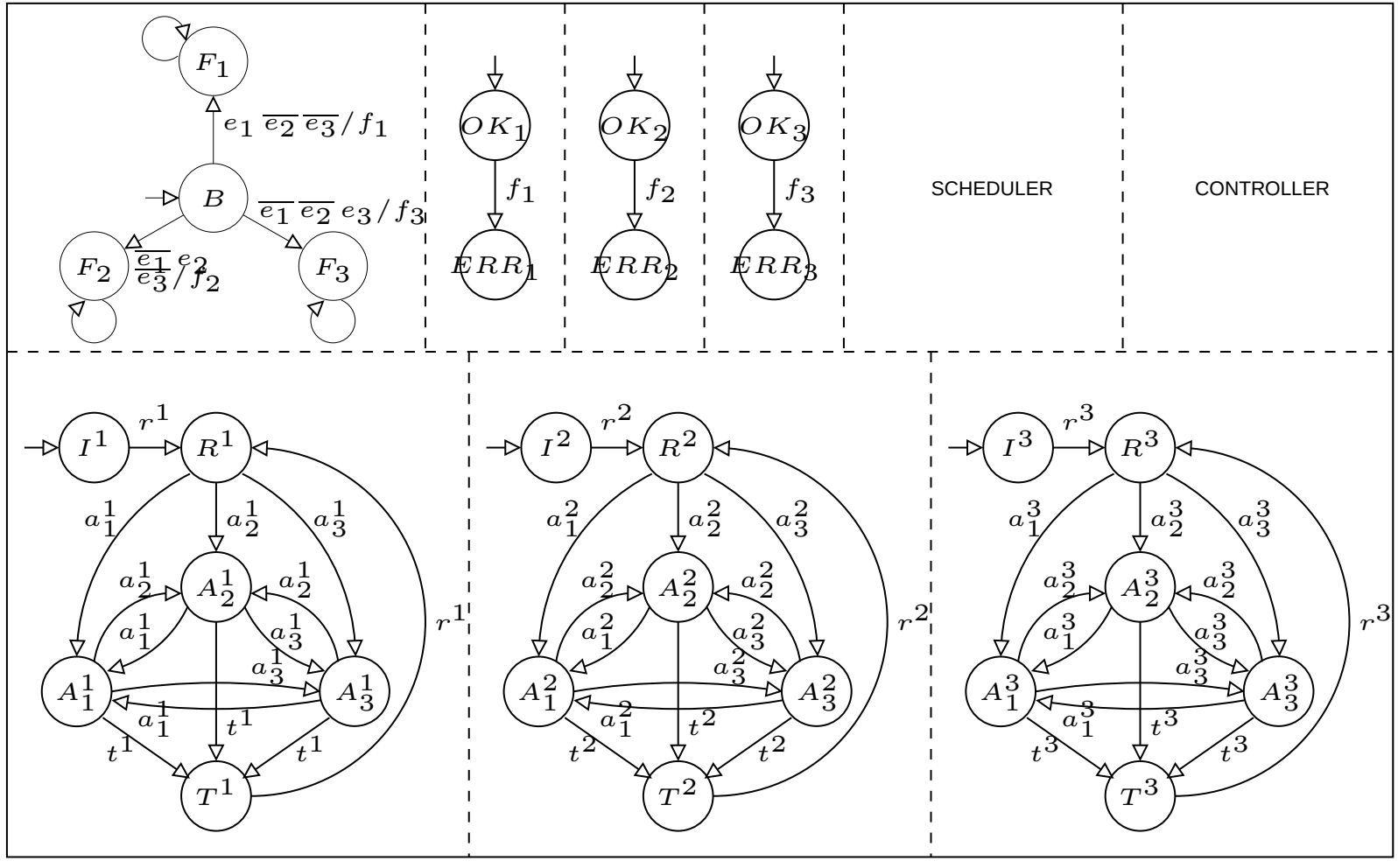
emitting requests in sequence

according to precedence graph



System model



composition of all that → the system to be controlled

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Order of synthesis operations essential: *not commutative*

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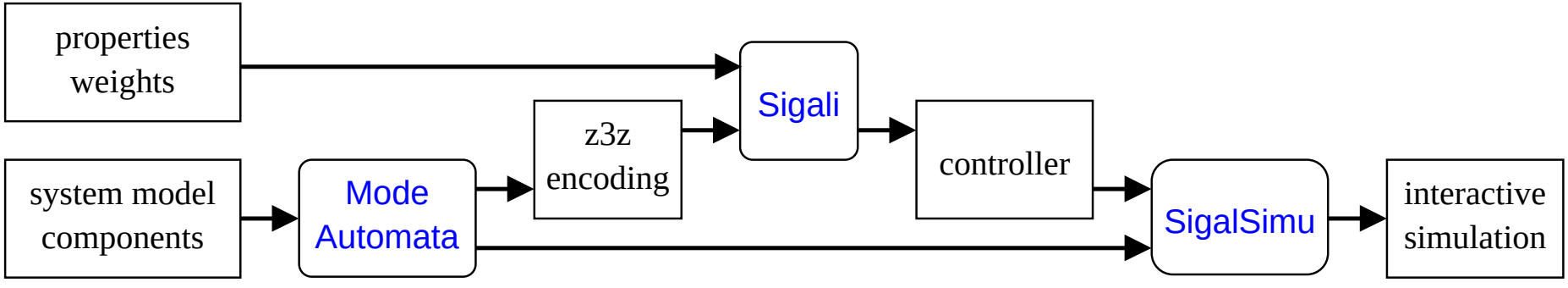
Optimizing costs and qualities: different solutions

when minimizing cost first, maximizing quality then

Implementation

Using synchronous tools



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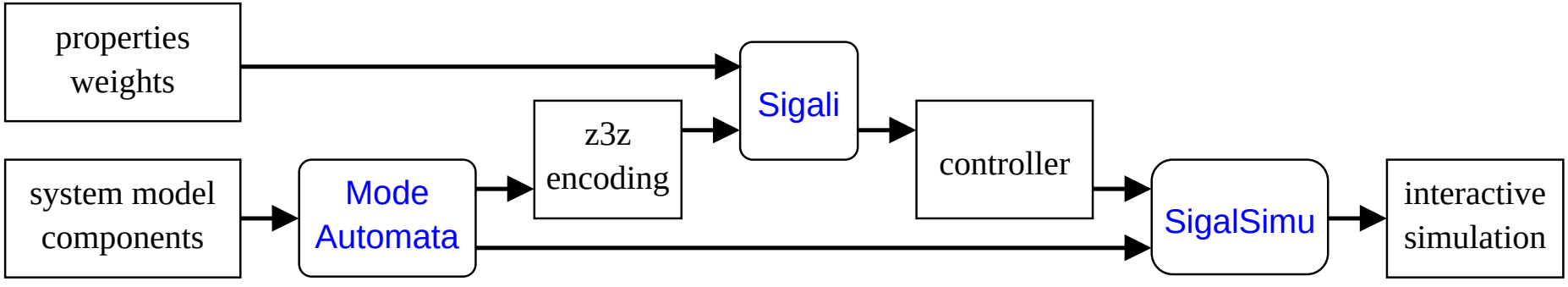

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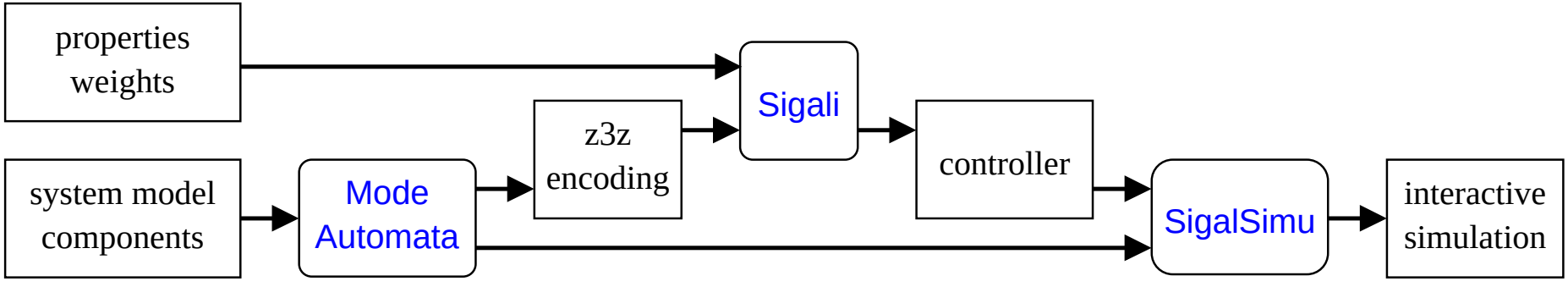

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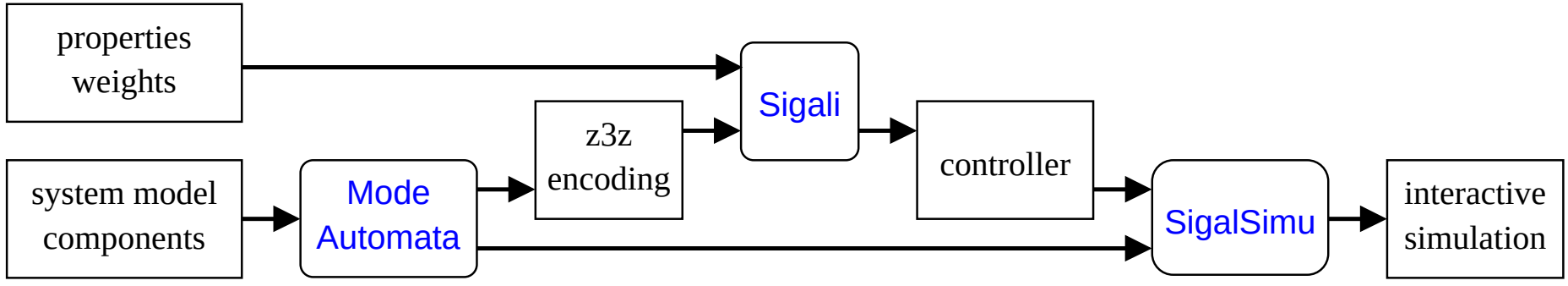
- objectives and synthesis with Sigali (IRISA)
- co-simulation with SigalSimu



Conclusion and perspectives

Results

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a formal model of a real-time distributed system
processors, faults, tasks, and reconfigurations

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POP ART

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model of tasks with modes, other architectures, ...

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- a formal model of a real-time distributed system
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Perspectives

- model of tasks with modes, other architectures, ...
- properties: exclusions on resources, observers, ...
- platform-based design: same system
  used under different control objectives

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