Verimag 20th Anniversary

Programme

Wednesday, September 26
- 13:30-14:00. Welcome coffee
  ● 14:00-15:00 — Joseph Sifakis — EPFL and Verimag — Rigorous System Design in BIP
  ● 15:00-16:00 — Ahmed Bouajjani — LIAFA, Paris — Analyzing Concurrent Program Behaviors under Weak Memory Models
- 16:00-16:30. Break
  ● 16:30-17:30 — Reinhard Wilhelm — Saarland University — Embedded Systems: Many Cores - Many Problems
- 18:00-20:00 – Welcome reception (UFR IM² AG)

Thursday, September 27
Morning session dedicated to Paul Caspi
  ● 9:00-10:00 — Albert Benveniste — IRISA/INRIA, Rennes — Semantics and Compilation of a Hybrid Language
  ● 10:00-11:00 — Gérard Berry — INRIA and Collège de France — Synchronous / Asynchronous Web Orchestration with Hop and HipHop
- 11:00-11:30. Break
  ● 11:30-12:30 — Matthieu Moy — Verimag — Transaction-Level Models of Systems-on-a-Chip Can they be Correct, Faithful and Fast?
- 12:30-14:00. Lunch
  ● 14:00-15:00 — Luca Benini — Università di Bologna — Digital Platform Design in the Twilight of Moore’s Law
  ● 15:00-16:00 — Gilles Barthe — IMDEA, Madrid — Computer-Aided Cryptographic Proofs
- 16:00-16:30. Break
  ● 16:30-17:30 — Jannik Dreier — Verimag — Computed-Aided Provable Security
- 19:30. Workshop dinner (restaurant “Chez le Per’Gras”)

Friday, September 28
  ● 9:00-10:00 — Pravin Varaiya — Berkeley University — The Max-Pressure Controller for Networks of Signalized Intersections
  ● 10:00-11:00 — Tom Henzinger — IST Austria — Twenty Years of Real-Time and Hybrid Systems
- 11:00-11:30. Break
  ● 11:30-12:30 — Oded Maler — Verimag — Timed Systems: The Unconquered Frontier
- 12:30. Lunch - End of the workshop