Validation of Systems-on-a-Chip at the Transactional Level
STMicroelectronics/UJF–VERIMAG Common Lab
openTLM: a Minalogic project
UJF–VERIMAG / Synchrone
STMicroelectronics HPC / SPG Group

Systems-on-a-Chip

Transaction-Level Modeling for the Development of Systems-on-a-Chip

Transaction Level Models (TLM)
- Pure Functional Models (PV: Programmer’s View)
- Performance Evaluation Models (PVT: Programmer’s View + Time)

C++/SystemC: a Standard for TLM Design
A SystemC program contains:
- The architecture of the SoC
- The embedded software
- The description of the hardware elements

PVT = PV + T?

VERIMAG/ST Joint Work

Challenges:
- Validation of Functional Properties at the TLM Level (test, formal verification)
- Estimation of Non-Functional Properties at the TLM Level (Time, Energy, ...)
- Formal Comparison Between levels of Abstraction
- Design methodologies for Refining Models (PVT from PV, ...)

The SystemC Simulation Tool:
- A Non-Preemptive Scheduler

The Dependency Analyser and Partial-Order Generator

Instrumented Model for the Partial-Order-Based Testing Method

Pinapa: an open-source SystemC parser

RVT: The Dependency Analyser and Partial-Order Generator

A Semantic Extractor

Lussy

Skelleton of the PVT Model

SystemC simulation tool

Lussy: A Semantic Extractor

new schedulings and timings

Registered Transfer level Models (RTL)

Synthesizable +
Very Detailed (data and cycle-accurate) +/-
Late Availability –
Slow Simulations –

Fast Simulations
Early Availability
Not Synthesizable
Very Abstract
Component-Based
Allow Early Development of the Embedded Software

VERIMAG/ST Joint Work

Third-Party Tools
SMV, nuSMV

Verification Tools
VERIMAG
Lesar, Nbac, IF

Lustre

Translator

Lustre Simulation Tools

Transaction Level Models (TLM)
- Pure Functional Models (PV: Programmer’s View)
- Performance Evaluation Models (PVT: Programmer’s View + Time)

No automatic transformations